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(54) SEMICONDUCTOR DEVICE

(57) A semiconductor device in which a transistor can supply an accurate current to a load (EL pixel and signal line) without being influenced by variations is provided.

A voltage at each terminal of a transistor is adjusted by a feedback circuit using an amplifier circuit. A current Idata is input from a current source circuit to the transistor, and a gate-source voltage is set by the feedback circuit so that the transistor can flow the current Idata. The feedback circuit controls the transistor to operate in a saturation region. Thus, a gate voltage required for flowing the current Idata is set.

With the use of the set transistor, a current can be supplied to a load (EL pixel and signal line) with accuracy. Note that a desired gate voltage can be set quickly since the amplifier circuit is utilized.

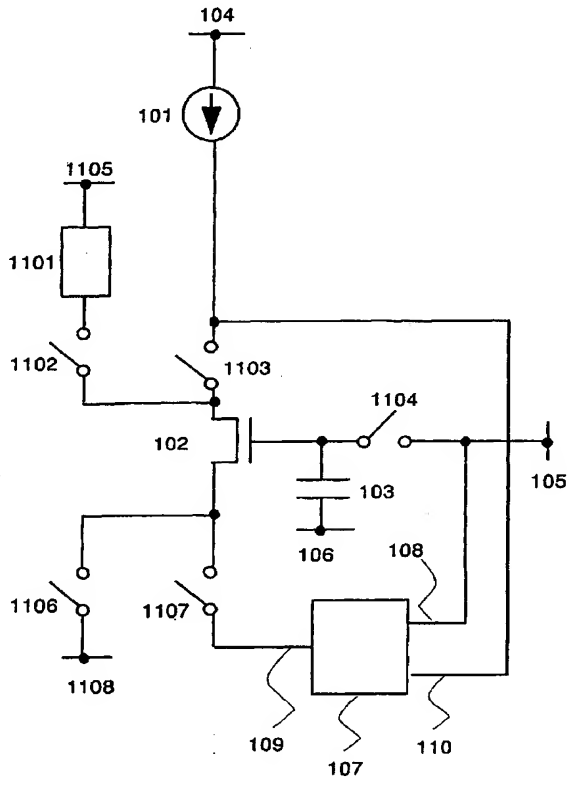

FIG. 11

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Description

TECHNICAL FIELD

[0001] The present invention relates to a semiconductor device provided with a function for controlling a current supplied to a load by a transistor. In particular, the invention relates to a semiconductor device that includes a pixel having a current-driven light emitting element whose luminance varies depending on a current and a signal line driver circuit for driving the pixel.

BACKGROUND ART

[0002] In recent years, a so-called self luminous type display device that includes a pixel having a light emitting element such as a light emitting diode (LED) attracts attention. As a light emitting element used for such a self luminous type display device, an organic light emitting diode (also called an OLED, an organic EL element, an electro luminescence (EL) element, or the like) draws attention and has been used for an organic EL display and the like.

[0003] Since a light emitting element such as an OLED is self luminous type, it does not require a backlight, and has the advantages of higher visibility of pixels, faster response and the like as compared with a liquid crystal display. Luminance of a light emitting element is controlled by a current value flowing into it.

[0004] As a driving method of a display device using such a self luminous type light emitting element, a passive matrix method and an active matrix method are known. The former has a problem in that a large and high luminance display cannot be realized easily, though its simple structure. Therefore, in recent years, the active matrix method has been actively developed, in which a current flowing into a light emitting element is controlled by thin film transistors (TFTs) provided in a pixel circuit.

[0005] In the case of a display device adopting such an active matrix method, there are problems in that a current flowing into a light emitting element changes due to variations in current characteristics of driving TFTs, resulting in variations in luminance.

[0006] That is, in the case of a display device adopting the active matrix method, driving TFTs for driving a current flowing into light emitting elements are used in a pixel circuit, and there are problems in that a current flowing into the light emitting elements changes due to variations in characteristics of these driving TFTs, resulting in variations in luminance. Thus, suggested are various circuits for suppressing variations in luminance, in which a current flowing into light emitting elements does not change even when characteristics of driving TFTs in a pixel circuit vary.

(Patent Document 1)
Patent Application Laid-Open No. 2002.517806
(Patent Document 2)
International Publication WO 01/06484
(Patent Document 3)
Patent Application Laid-Open No. 2002-514320
(Patent Document 4)
International Publication WO 02/39420

[0007] A configuration of an active matrix display device is disclosed in Patent Documents 1 to 4. Disclosed in Patent Documents 1 to 3 is a circuit configuration in which a current flowing into light emitting elements does not change due to variations in characteristics of driving TFTs disposed in a pixel circuit. This configuration is called a current writing pixel or a current input pixel. Meanwhile, disclosed in Patent Document 4 is a circuit configuration for suppressing changes in signal current due to variations in TFTs in a source driver circuit.

[0008] FIG. 6 shows a first configuration example of an existing active matrix display device that is disclosed in Patent Document 1. A pixel shown in FIG. 6 comprises a source signal line 601, first to third gate signal lines 602 to 604, a current supply line 605, TFTs 606 to 609, a capacitor element 610, an EL element 611, and an image signal inputting current source 612.

[0009] A gate electrode of the TFT 606 is connected to the first gate signal line 602, a first electrode thereof being connected to the source signal line 601 and a second electrode thereof being connected to a first electrode of the TFT 607, a first electrode of the TFT 608 and a first electrode of the TFT 609. A gate electrode of the TFT 607 is connected to the second gate signal line 603, a second electrode thereof being connected to a gate electrode of the TFT 608. A second electrode of the TFT 608 is connected to the current supply line 605. A gate electrode of the TFT 609 is connected to the third gate signal line 604, a second electrode thereof being connected to an anode of the EL element 611. The capacitor element 610 is connected between the gate electrode of the TFT 608 and the current supply line, and holds a gate-source voltage of the TFT 608. The current supply line 605 and a cathode of the EL element 611 are input with respective predetermined potentials and have a potential difference therebetween.

[0010] Operations from writing of a signal current to light emission are described with reference to FIGS. 7A to 7E. Each component in the drawings is denoted by the same reference numeral as FIG. 6. FIGS. 7A to 7C are schematic diagrams each showing a current flow. FIG. 7D shows a relationship between currents flowing in each path in writing a signal current. FIG. 7E shows a voltage that is held in the capacitor element 610 in writing a signal current also, namely the gate-source voltage of the TFT 608.

[0011] First, a pulse is input to the first gate signal line 602 and the second gate signal line 603, thereby the TFTs 606 and 607 are turned on. A current flowing in the source signal line 601 at this time, namely a signal current is referred to as Idata.

[0012] Since the current Idata flows in the source sig-

nal line 601, a current flows in a pixel through current paths I1 and I2 as shown in FIG. 7A. The relationship between the divided currents is shown in FIG. 7D. It is needless to say that Idata = 11 + I2 is satisfied.

[0013] At the moment when the TFT 606 is turned on, electric charges have not been held in the capacitor element 610 yet, thus the TFT 608 is off. Accordingly, 12 is equal to 0 whereas Idata is equal to I1. That is, during this period, a current flows only to be accumulated in the capacitor element 610.

[0014] Then, electric charges are slowly accumulated in the capacitor element 610, and thereby a potential difference begins to occur between both electrodes (FIG. 7E). When a potential difference between both electrodes being equal to Vth (FIG. 7E, point A), the TFT 608 is turned on and I2 is generated. Since Idata = I1 + 12 is satisfied as described above, I1 gradually decreases, though a current flows yet and electric charges are further accumulated in the capacitor element.

[0015] In the capacitor element 610, electric charges continue to be accumulated until a potential difference between both electrodes thereof, that is, the gate-source voltage of the TFT 608 becomes equal to a desired voltage, namely a voltage (Vgs) that allows the TFT 608 to supply the current Idata. When the accumulation of electric charges is completed (FIG. 7E, point B), the current I1 stops flowing, the TFT 608 supplies a current corresponding to the Vgs at this time, and thereby Idata becomes equal to I2 (FIG. 7B). Thus, the steady state is reached. That is the end of the writing operation of signals. Finally, the selection of the first gate signal line 602 and the second gate signal line 603 is completed and the TFT_s 606 and 607 are turned off.

[0016] Subsequently, a light emitting operation starts. A pulse is input to the third gate signal line 604, thereby the TFT 609 is turned on. Since the capacitor element 610 holds the Vgs that has been written earlier, the TFT 608 is on and the current Idata is supplied from the current supply line 605. Accordingly, the EL element 611 emits light. When the TFT 608 is set to operate in a saturation region at this time, the current Idata can flow without changes even when a source-drain voltage of the TFT 608 varies.

[0017] Such an operation that outputs a set current is called an output operation herein. The current writing pixel shown above as an example has the advantages that even when there are variations in characteristics and the like of the TFT 608, the capacitor element 610 holds a gate-source voltage required for flowing the current Idata, a desired current can be supplied to the EL element with accuracy, thereby variations in luminance due to variations in characteristics of TFTs can be suppressed.

[0018] Described above is an example for correcting changes in current due to variations of driving TFTs in a pixel circuit. The same problem occurs in a source driver circuit. Disclosed in Patent Document 4 is a circuit configuration for preventing changes in signal current due to production variations of TFTs in a source driver circuit.

(Patent Document 5)
Patent Application Laid-Open No. 2003-108069

[0019] Furthermore, another method than those shown in Patent Documents 1 to 4 is disclosed in Patent Document 5. A configuration diagram thereof is shown in FIG. 44. FIG. 44 shows a driver circuit of a light emitting element, which includes a current supply circuit (1) and a driver control circuit (2a). In the driver circuit shown in FIG. 44, a current (Is) that is equal to a current (Ir) supplied from a supply transistor (M5) for supplying a current to drive a light emitting element (EL) flows into the driver control circuit (2a) through a reference transistor (M4). Then, depending on the current (Is), source-drain voltage data (Vs) of the reference transistor (M4), and source-drain voltage data (Vr, Vdrv) of the supply transistor (M5), the current (Is) can be controlled to be close to a desired predetermined current value (Idrv) and each source-drain voltage data (Vs, Vr) can be controlled to be equal to each other.

DISCLOSURE OF THE INVENTION

(Problems to be Solved by the Invention)

[0020] As set forth above, in the conventional technologies, a circuit is configured so that a signal current and a current for driving a TFT, or a signal current and a current flowing into a light emitting element in light emission may be equal or proportional to each other.

[0021] However, parasitic capacitance of a wiring used for supplying a signal current to a driving TFT and a light emitting element is considerably large. Therefore, there are problems in that in the case of a signal current being small, the time constant for charging parasitic capacitance of a wiring is increased, and thereby signal writing speed becomes slower. That is, the problem is that it takes a long time to develop at a gate terminal a voltage required for flowing a signal current supplied to a transistor, and signal writing speed becomes slower.

[0022] Furthermore, in the case of the configuration shown in FIG. 44, a transistor M7 and a transistor M9 need to have the same current characteristics. Variations In current characteristics lead to variations in current flowing into a light emitting element (EL). Similarly, a transistor M8 and a transistor M11, a transistor M10 and a transistor M12, and the like need to have the same current characteristics. In this manner, many transistors need to have the same current characteristics because variations in current characteristics lead to variations in current flowing into a light emitting element (EL). In addition, as seen by comparison of FIG. 44 and FIG. 6, the circuit in FIG. 44 has much more transistors and a more complicated configuration. Accordingly, reduced productive yield, increased cost, enlarged layout of circuit, and increased power consumption may occur.

[0023] In view of the foregoing problems, it is an object of the invention to provide a semiconductor device that

can reduce the influences of variations in characteristics of transistors, and improve signal writing speed sufficiently even in the case of a signal current being small.

(Means for Solving the Problems)

[0024] In order to achieve the aforementioned object, according to the invention, a potential of a transistor that supplies a current to a load is controlled by an amplifier circuit, and a potential of a source or a drain of the transistor is stabilized by constituting a feedback circuit.

[0025] A semiconductor device of the invention is characterized by having a circuit in which a current supplied to a load is controlled by a transistor whose source or drain is connected to a current source circuit, and an amplifier circuit for controlling a source potential or a drain potential of the transistor so that the transistor may operate in a saturation region when a current is supplied from the current source circuit to the transistor.

[0026] A semiconductor device of the invention is characterized by having a circuit in which a current supplied to a load is controlled by a transistor whose source or drain is connected to a current source circuit, and an amplifier circuit for stabilizing a source potential or a drain potential of the transistor.

[0027] A semiconductor device of the invention is characterized by having a circuit in which a current supplied to a load is controlled by a transistor whose source or drain is connected to a current source circuit, and a feedback circuit for stabilizing a source potential or a drain potential of the transistor.

[0028] A semiconductor device of the invention is characterized by having a transistor for controlling a current supplied to a load and an operational amplifier, wherein an inverting input terminal of the operational amplifier is connected to a drain terminal side of the transistor connected to a current source circuit, a non-inverting input terminal of the operational amplifier is connected to a gate terminal side of the transistor, and an output terminal of the operational amplifier is connected to a source terminal side of the transistor.

[0029] A semiconductor device of the invention is characterized by having a transistor for controlling a current supplied to a load and an operational amplifier, wherein an inverting input terminal of the operational amplifier is connected to a drain terminal side of the transistor connected to a current source circuit, a non-inverting input terminal of the operational amplifier is connected to a gate terminal side of the transistor, and an output terminal of the operational amplifier is connected to the drain terminal side of the transistor.

[0030] A semiconductor device of the invention is characterized by having a transistor for controlling a current supplied to a load and a voltage follower circuit, wherein an input terminal of the voltage follower circuit is connected to a gate terminal side of the transistor connected to a current source circuit, and an output terminal of the voltage follower circuit is connected to a drain terminal side of the transistor. In this configuration of the invention, the voltage follower circuit may be constituted by a source follower circuit.

[0031] In the invention, the type of applicable transistor is not especially limited, and a thin film transistor (TFT) using a non-single crystalline semiconductor film typified by amorphous silicon and polycrystalline silicon, a MOS transistor formed by using a semiconductor substrate or an SOI substrate, a junction transistor, a transistor using an organic semiconductor or a carbon nanotube, and other transistors may be employed. Further, the type of substrate on which a transistor is disposed is not especially limited, and the transistor may be formed on a single crystalline substrate, an SOI substrate, a glass substrate, or the like.

[0032] Note that in the invention, connection means electrical connection. Accordingly, other elements, switch and the like may be disposed therebetween.

(Effect of the Invention)

[0033] According to the invention, a feedback circuit is constituted by an amplifier circuit in order to control a transistor. As a result, the transistor can output a constant current without being influenced by variations. Such a set operation can be carried out quickly since the amplifier circuit is used. Thus, an accurate current can be output in an output operation. In addition, the amplifier circuit allows a set operation to be carried out with accuracy even when current characteristics vary. Therefore, the amplifier circuit can be easily constituted by transistors such as TFTs with large variations in current characteristics.

BRIEF DESCRIPTION OF THE DRAWINGS

[0034]

FIG. 1 shows a structure of a semiconductor device of the invention.
FIG. 2 shows a structure of a semiconductor device of the invention.
FIG. 3 shows a structure of a semiconductor device of the invention.
FIG. 4 shows a structure of a semiconductor device of the invention.
FIG. 5 shows a structure of a semiconductor device of the invention.
FIG. 6 shows an existing pixel configuration.
FIGS. 7A to 7E shows operations of an existing pixel.
FIG. 8 shows a structure of a semiconductor device of the invention.
FIG. 9 shows a structure of a semiconductor device of the invention.
FIG. 10 shows a structure of a semiconductor device of the invention.
FIG. 11 shows a structure of a semiconductor device of the invention.

FIG. 12 shows an operation of a semiconductor device of the invention.
FIG. 13 shows an operation of a semiconductor device of the invention.
FIG. 14 shows an operation of a semiconductor device of the invention.
FIG. 15 shows an operation of a semiconductor device of the invention.
FIG. 16 shows an operation of a semiconductor device of the invention.
FIG. 17 shows an operation of a semiconductor device of the invention.
FIG. 18 shows a structure of a semiconductor device of the invention.
FIG. 19 shows a structure of a semiconductor device of the invention.
FIG. 20 shows an operation of a semiconductor device of the invention.
FIG. 21 shows an operation of a semiconductor device of the invention.
FIG. 22 shows an operation of a semiconductor device of the invention.
FIG. 23 shows a structure of a semiconductor device of the invention.
FIG. 24 shows a structure of a semiconductor device of the invention.
FIG. 25 shows a structure of a semiconductor device of the invention.
FIG. 26 shows a structure of a semiconductor device of the invention.
FIG. 27 shows an operation of a semiconductor device of the invention.
FIG. 28 shows an operation of a semiconductor device of the invention.
FIG. 29 shows a structure of a semiconductor device of the invention.
FIG. 30 shows a structure of a semiconductor device of the invention.
FIG. 31 shows a structure of a semiconductor device of the invention.
FIG. 32 shows a structure of a semiconductor device of the invention.
FIG. 33 shows a structure of a semiconductor device of the invention.
FIG. 34 shows a structure of a semiconductor device of the invention.
FIG. 35 shows a structure of a semiconductor device of the invention.
FIG. 36 shows a structure of a semiconductor device of the invention.
FIG. 37 shows a structure of a semiconductor device of the invention.
FIG. 38 shows a structure of a display device of the invention.
FIG. 39 shows a structure of a display device of the invention.
FIG. 40 shows an operation of a display device of the invention.
FIG. 41 shows an operation of a display device of the invention.
FIG. 42 shows an operation of a display device of the invention.
FIGS. 43A to 43H shows electronic appliances to which the invention is applied.
FIG. 44 shows an existing pixel configuration.

BEST MODE FOR CARRYING OUT THE INVENTION

[0035] Embodiment modes of the invention will be described hereinafter with reference to the accompanying drawings. However, it is to be understood that various changes and modifications will be apparent to those skilled in the art. Therefore, unless such changes and modifications depart from the scope of the invention, they should be constructed as being included therein.

(Embodiment Mode 1)

[0036] According to the invention, a pixel comprises an element whose luminance can be controlled by a current value flowing into a light emitting element. Typically, an EL element can be adopted. Although various configurations of an EL element are known, any configuration of an EL element can be used in the invention as long as the luminance can be controlled by a current value. In other words, an EL element may be formed by freely combining a light emitting layer, an electron transporting layer, or an electron injection layer. As a material for forming an EL element, a low molecular weight organic material, a medium molecular weight organic material (an organic light emitting material that does not have subliming property and that has a molecular number of 20 or less, or a length of chained molecules of 10 μm or less), or a high molecular weight organic material may be employed. Alternatively, an inorganic material may be mixed or dispersed into these organic materials.

[0037] The invention can be applied to various analog circuits having a current source as well as to a pixel having a light emitting element such as an EL element. Thus, in this embodiment mode, the principle of the invention is described.

[0038] FIG. 1 shows a configuration based on the basic principle of the invention. A current source circuit 101 and a current source transistor 102 are connected to a wiring 104. FIG. 1 shows the case in which a current flows from the current source circuit 101 to the current source transistor 102. A first input terminal 108 of an amplifier circuit 107 is connected to a gate terminal of the current source transistor 102. A second input terminal 110 of the amplifier circuit 107 is connected to a drain terminal of the current source transistor 102. An output terminal 109 of the amplifier circuit 107 is connected to a source terminal of the current source transistor 102. Moreover, the gate terminal of the current source transistor 102 is connected to a wiring 105.

[0039] A capacitor element 103 is connected to the

gate terminal of the current source transistor 102 and a wiring 106 in order to hold a gate voltage of the current source transistor 102. It is to be noted that the capacitor element 103 can be omitted when gate capacitance of the current source transistor 102, or the like is used instead.

[0040] In such a configuration, a current Idata is supplied and input from the current source circuit 101 and the current Idata flows into the current source transistor 102. The amplifier circuit 107 controls so that the current Idata supplied from the current source circuit 101 may flow into the current source transistor 102 and the steady state may be reached during a period in which the current source transistor 102 operates in a saturation region. Thus, a source potential of the current source transistor 102 is set to a level at which the current source transistor 102 can flow the current Idata. That is, the source potential of the current source transistor 102 is controlled so that a gate-source voltage may be set to a level at which the current source transistor 102 can flow the current Idata. At this time, the source potential of the current source transistor 102 is set to a proper value independently of current characteristics (mobility, threshold voltage and the like) and size (gate width W and gate length L) of the current source transistor 102. Therefore, even when there are variations in current characteristics and size of the current source transistor 102, the current source transistor 102 can supply the current Idata. As a result, the current source transistor 102 can operate as a current source and supply a current to various loads (another current source transistor, a pixel, a signal line driver circuit, and the like).

[0041] Since the output impedance of the amplifier circuit 107 is not high, a large current can be output. Thus, the source terminal of the current source transistor 102 can be charged quickly. In other words, writing of the current Idata can be carried out faster to be completed quickly, and thereby it takes a short time to reach the steady state.

[0042] An operation of the amplifier circuit 107 is described next. The amplifier circuit 107 has a function to detect voltages of the first input terminal 108 and the second input terminal 110, and amplify the input voltages to be output to the output terminal 109. In FIG. 1, the second input terminal 110 and the output terminal 109 are connected through the source and the drain of the current source transistor 102, namely they constitute a feedback circuit. Because of the feedback circuit, the voltage of the second input terminal 110 changes depending on the voltages of the output terminal 109 and the first input terminal 108 (the gate terminal of the current source transistor 102), and the voltage of the output terminal 109 changes also depending on the voltage of the second input terminal 110. Through such a feedback operation, a voltage to stabilize the state of each input terminal can be output.

[0043] In FIG. 1, the gate terminal of the current source transistor 102 is connected to the first input terminal 108, the source terminal thereof being connected to the output terminal 109, and the drain terminal thereof being connected to the second input terminal 110. Accordingly, a voltage to stabilize the voltage between the drain terminal and the gate terminal of the current source transistor 102 is output to the source terminal of the current source transistor 102 by the amplifier circuit 107. At this time, the current Idata is supplied from the current source circuit 101 to the current source transistor 102. As a result, a voltage that allows the current source transistor 102 to supply the current Idata is output from the current source circuit 101 to the source terminal of the current source transistor 102. That is, a voltage is output to the source terminal of the current source transistor 102 so that a gate-source voltage may be set to a level at which the current source transistor 102 can flow the current Idata.

[0044] In general, an operating region of a transistor (an NMOS transistor is taken as an example herein for simplicity) can be divided into a linear region and a saturation region. The boundary between these regions is, when a drain-source voltage is Vds, a gate-source voltage is Vgs and a threshold voltage is Vth, a point at which (Vgs - Vth) = Vds is satisfied. In the case of (Vgs - Vth) > Vds being satisfied, a transistor operates in a linear region and a current value is determined by the Vds and the Vgs. On the other hand, in the case of (Vgs - Vth) < Vds being satisfied, a transistor operates in a saturation region and a current value does not change much even when the Vds varies. That is, the current value is determined only by the Vgs.

[0045] As is evident from the foregoing, the amplifier circuit 107 may control the current source transistor 102 to operate in a saturation region. According to this, the gate-source voltage of the current source transistor 102 is set to a voltage at which the current Idata can be supplied. In order that the current source transistor 102 operates in a saturation region, (Vgs - Vth) < Vds has only to be satisfied. The threshold voltage Vth of an N-channel transistor is generally more than 0, therefore, the potential of the drain terminal of the current source transistor 102 has to be equal to or more than the potential of the gate terminal. The amplifier circuit 107 controls the current source transistor 102 so as to achieve such an operation.

[0046] As set forth above, with the use of the feedback circuit including the amplifier circuit 107, the gate-source voltage of the current source transistor 102 can be set so as to flow as large a current as that supplied from the current source circuit 101. The set operation can be completed quickly because the amplifier circuit 107 is used, and thereby writing is completed in a short time. The set current source transistor 102 can operate as a current source circuit and supply a current to various loads.

[0047] Although FIG. 1 shows the case in which a current flows from the current source circuit 101 to the current source transistor 102, the invention is not limited to this. FIG. 2 shows the case in which a current flows from a current source transistor 202 to a current source circuit

201. As mentioned above, when the polarity of the current source transistor 202 is changed, it is possible to change the direction of current without modifying the connection of the circuit. Note that a reference numeral 203 denotes a capacitor element, 204 to 206 denote wirings, 207 denotes an amplifier circuit, 208 denotes a first input terminal, 209 denotes an output terminal, and 210 denotes a second input terminal.

[0048] Although an N-channel transistor is used for the current source circuit 101 in FIG. 1, the invention is not limited to this, and a P-channel transistor may be used as well. However, when the polarity of the transistor is changed without modifying the direction of current, a source terminal and a drain terminal are changed over. Therefore, the connection of the circuit has to be changed. A configuration in that case is shown in FIG. 3. The current source circuit 101 and a current source transistor 302 are connected to the wiring 104. FIG. 3 shows the case in which a current flows from the current source circuit 101 to the current source transistor 302, though the direction of current can be changed as the case shown in FIG. 2. The first input terminal 108 of the amplifier circuit 107 is connected to a gate terminal of the current source transistor 302. The second input terminal 110 of the amplifier circuit 107 is connected to a drain terminal of the current source transistor 302. The output terminal 109 of the amplifier circuit 107 is connected to the drain terminal of the current source transistor 302.

[0049] Accordingly, a voltage to stabilize the voltages of the drain terminal and the gate terminal of the current source transistor 302 is output to the drain terminal of the current source transistor 302 by the amplifier circuit 107. At this time, the current Idata is supplied from the current source circuit 101 to the current source transistor 302. As a result, a voltage at which the current source transistor 302 can supply the current Idata (in other words, a voltage required in order that the current source transistor 302 operates in a saturation region) is output from the current source circuit 101 to the drain terminal of the current source transistor 302. Then, a source potential of the current source transistor 302 is set so that a gate-source voltage may be a level at which the current source transistor 302 can supply the current Idata.

[0050] It is to be noted that in FIG. 1, the capacitor element 103 is only required to hold the gate potential of the current source transistor 102, thus a potential of the wiring 106 may be set arbitrarily. Therefore, potentials of the wiring 105 and the wiring 106 may be equal or different. However, a current value of the current source transistor 102 is determined by the gate-source voltage thereof. Accordingly, it is more preferable that the capacitor element 103 holds the gate-source voltage of the current source transistor 102, and the wiring 106 is thus preferably connected to the source terminal of the current source transistor 102. As a result, influences of wiring resistance and the like can be suppressed.

[0051] Sirnilarly in FIG. 2, it is desirable that a wiring 206 be connected to a source terminal of the current source transistor 202. Furthermore, in FIG. 3, the wiring 106 is preferably connected to a source terminal of the current source transistor 302.

(Embodiment Mode 2)

[0052] Shown in Embodiment Mode 2 is an example of the amplifier circuit used in FIGS. 1 to 3.

[0053] First, an operational amplifier is taken as an example of the amplifier circuit. FIG. 4 is a configuration diagram corresponding to FIG. 1, which shows the case of adopting an operational amplifier as an amplifier circuit. The first input terminal 108 of the amplifier circuit 107 corresponds to a non-inverting (positive phase) input terminal of an operational amplifier 407 whereas the second input terminal 110 corresponds to an inverting input terminal.

[0054] The operational amplifier normally operates so that a potential of a non-inverting (positive phase) input terminal may be equal to a potential of an inverting input terminal. Accordingly, in FIG. 4, the source potential of the current source transistor 102 is controlled so that the gate potential of the current source transistor 102 may be equal to the drain potential thereof. Thus, Vgs = Vds is satisfied, and thereby the current source transistor 102 operates in a saturation region in the case of Vth being more than 0.

[0055] Similarly to FIG. 4, FIG. 5 shows a configuration diagram corresponding to FIG. 2 and FIG. 8 shows a configuration diagram corresponding to FIG. 3. Reference numeral 507 denotes an operational amplifier herein.

[0056] In the case of FIG. 8, the drain potential of the current source transistor 302 is controlled so that the gate potential of the current source transistor 302 may be equal to the drain potential thereof. Since the gate potential and the drain potential are equal to each other, Vgs = Vds is satisfied, and thereby the current source transistor 302 operates in a saturation region in the case of Vth being more than 0.

[0057] It is to be noted that any type of operational amplifier may be used as the operational amplifier used in FIG. 4, FIG. 5, and FIG. 8. A voltage feedback operational amplifier or a current feedback operational amplifier may be used. Alternatively, an operational amplifier added with various correction circuits such as a phase compensation circuit may be employed.

[0058] The operational amplifier normally operates so that a potential of a non-inverting (positive phase) input terminal may be equal to a potential of an inverting input terminal, though the potentials of the non-inverting (positive phase) input terminal and the inverting input terminal may not be equal due to variations in characteristics and the like. In other words, an offset voltage may be generated. In that case, similarly to a normal operational amplifier, potentials of a non-inverting (positive phase) input terminal and an inverting input terminal may be adjusted

to be equal to each other. In the case of the invention, however, the current source transistor 102 is only required to be controlled to operate in a saturation region. Therefore, as long as the current source transistor 102 operates in a saturation region, an offset voltage may be generated in the operational amplifier and variations in offset voltages do not have an effect. Accordingly, even when the operational amplifier is constituted by transistors whose current characteristics vary significantly, it can operate normally.

[0059] When focusing on the connection of the circuit shown in FIG. 8, the second input terminal 110 of the operational amplifier (inverting input terminal) is connected to the output terminal 109. This circuit configuration is generally called a voltage follower circuit. That is, a voltage of the first input terminal 108 (the non-inverting (positive phase) input terminal) is output to the output terminal, and the input and output impedance is converted. Therefore, not only the operational amplifier connected as shown in FIG. 8 but also a circuit having a function similar to the voltage follower circuit may be utilized as the amplifier circuit 107 used in FIG. 3.

[0060] There is a source follower circuit as a circuit for converting the input and output impedance. In a normal source follower circuit, an input potential and an output potential are not equal to each other. However, in the amplifier circuit 107 used in FIG. 3, the input potential and the output potential thereof are not required to be equal to each other. That is, the amplifier circuit has to be a circuit that can control the current source transistor 302 to operate in a saturation region. Thus, FIG. 9 shows a configuration in the case of using a source follower circuit 907 as the amplifier circuit 107. When a potential of an input terminal 908 (gate terminal of an amplifying transistor 901), namely a potential of the gate terminal of the current source transistor 302 changes, a potential of the output terminal 109 (source terminal of the amplifying transistor 901), namely a potential of the drain terminal of the current source transistor 302 also changes. When the potential of the drain terminal of the current source transistor 102 changes, a potential of the source terminal of the current source transistor 302 also changes.

[0061] In FIG. 9, an N-channel transistor is used as the amplifying transistor 901. Accordingly, the potential of the output terminal 109 (source terminal of the amplifying transistor 901) is lower than the potential of the input terminal 908 (gate terminal of the amplifying transistor 901) by a gate-source voltage of the amplifying transistor 901. Thus, the current source transistor 302 operates in a saturation region. As is evident from the foregoing, in the case of a source follower circuit 907 being used as the amplifying circuit 107 in FIG. 3, it is preferable to adopt a configuration in which the current source transistor 302 can operate in a saturation region easily (in the case of FIG. 9, the amplifying transistor 901 is an N-channel transistor). However, a P-channel transistor may be employed for the amplifying transistor 901 in FIG. 9, as long as it operates normally. FIG. 10 shows a configuration diagram corresponding to FIG. 9, in which the direction of current is inverted. As shown in FIG. 10, the polarity of each transistor may be changed.

[0062] Although biasing transistors 902 and 1002 are used and a bias voltage is applied to gate terminals thereof 903 and 1003 in FIG. 9 and FIG. 10, the invention is not limited to this. A resistor element and the like may be used instead of the biasing transistors 902 and 1002. Alternatively, a push-pull circuit may be constituted by a transistor that has the opposite polarity to amplifying transistors 901 and 1001.

[0063] In the case of source follower circuits 907 and 1007, similarly to the case of the operational amplifier, variations in output voltages do not have an effect as long as the current source transistors 302 and 10002 operate in a saturation region. Accordingly, even when the source follower circuits 907 and 1007 are constituted by transistors whose current characteristics vary significantly, it can operate normally.

[0064] As described above, as long as the current source transistor operates in a saturation region, variations in output voltages of the amplifier circuit do not have an effect. Therefore, in the voltage follower circuit, the source follower circuit and the like, an input voltage does not have to be proportional to an output voltage. That is, any circuit may be adopted as long as the current source transistor can be controlled to operate in a saturation region.

[0065] As set forth above, as long as the current source transistors 102, 202, 302, and 1002 operate in a saturation region, variations in characteristics of the amplifier circuits 107 and 207, the operational amplifiers 407 and 507, and the source follower circuits 907 and 1007 used in FIGS. 1 to 5 and FIGS. 8 to 10 do not have an effect. Therefore, even in the case of the amplifier circuits 107 and 207, the operational amplifiers 407 and 507, and the source follower circuits 907 and 1007 being constituted by transistors whose current characteristics vary significantly, a normal operation can be performed.

[0066] Accordingly, a thin film transistor (including a transistor using amorphous or polycrystalline as an active layer), an organic transistor or the like may be effectively used instead of a transistor whose channel portion is formed of single crystalline.

[0067] Although the operational amplifier and the source follower circuit are used as an example of the amplifier circuits 107 and 207, the invention is not limited to this. The amplifier circuit can be constituted by other various circuits such as a differential circuit, a common drain amplifier circuit and a common source amplifier circuit.

[0068] It is to be noted that the description in this embodiment mode corresponds to a detailed description of a part of the configuration shown in Embodiment Mode 1. However, various changes and modifications are possible unless such changes and modifications depart from the scope of the invention.

(Embodiment Mode 3)

[0069] According to the invention, a current Idata is supplied from a current source circuit, and a current source transistor is set to flow the current Idata. Then, the set current source transistor operates as a current source circuit and supplies a current to various loads. Described in this embodiment are a connection between a load and a current source transistor, a configuration of a transistor when supplying a current to a load, and the like.

[0070] Although this embodiment mode will be described, for simplicity, with reference to the configuration shown in FIG. 1, and more particularly the configuration using the operational amplifier 407 as the amplifier circuits 107 and 207 (FIG. 4), the invention is not limited to this. This embodiment mode can be easily applied to other configurations as shown in FIGS. 2 to 5, FIGS. 8 to 10 and the like.

[0071] In addition, described in this embodiment mode is the case where a current flows from the current source circuit to the current source transistor and the current source transistor is an N-channel transistor, though the invention is not limited to this. This embodiment mode can be easily applied to other configurations as shown in FIGS. 2 to 5, FIGS. 8 to 10 and the like.

[0072] First, FIG. 11 shows a configuration in which a current is supplied to the load 1101 by using only the current source transistor 102 to which a current is supplied from the current source circuit 101.

[0073] Note that any type of load can be employed. It may be an element such as a resistor, a transistor, an BL element, other light emitting elements, a current source circuit including a transistor, a capacitor, a switch and the like, and a wiring connected to a certain circuit. In addition, a signal line may be used as well as a signal line and a pixel connected thereto. The pixel may comprise any display element such as an EL element and an element used for FED.

[0074] An operation of FIG. 11 is described taking for example the case of an operational amplifier being used as the amplifier circuit 107. First, as shown in FIG. 12, switches 1103, 1104 and 1107 are turned on. Then, an operational amplifier 407 controls a source potential of the current source transistor 102 so that the current source transistor 102 may flow a current Idata supplied from the current source circuit 101 while operating in a saturation region. Since the operational amplifier 407 is used at this time, writing can be carried out quickly. Subsequently, the switch 1104 is turned off as shown in FIG. 13, and thereby the gate potential of the current source transistor 102 is held in the capacitor element 103. When the switches 1103 and 1107 are turned off as shown in FIG. 14, current supply is stopped. Then, switches 1102 and 1106 are turned on as shown in FIG. 15, and thereby a current is supplied to a load 1101. The amount of current at this time is equal to the Idata when the current source transistor 102 operates in a saturation region. That is, even when there are variations in current characteristics and size of the current source transistor 102, influences thereof can be prevented.

[0075] In the case of the wiring 106 being added with a certain potential, the source potential of the current source transistor 102 in writing and setting a current (FIG. 12) may differ from that in outputting a current (FIG. 15). In that case, the gate-source voltage of the current source transistor 102 may vary. Variation of the gate-source voltage leads to variation of a current value. Thus, the gate-source voltage in writing and setting a current (FIG. 12) has to be equal to that in outputting a current (FIG. 15). In order to achieve this, for instance, the wiring 106 may be connected to the source terminal of the current source transistor 102. Accordingly, the gate-source voltage can be kept constant even when the source potential of the current source transistor 102 varies, since the gate potential varies depending on the variation of the source potential.

[0076] Alternatively, a potential of the wiring 1108 may be controlled so as to be equal to an output potential of the operational amplifier 407 in writing and setting a current. For instance, a voltage follower circuit or the like may be connected to the wiring 1108 to control the potential of the wiring 1108.

[0077] Instead, as shown in FIGS. 16 and 17, a capacitor element 1603 may be disposed between the second input terminal 110 and the wiring 1106, and electric charges may be held by a switch 1604, thereby a current may be supplied from the operational amplifier 407 in outputting a current (FIG. 17) as well as in writing and setting a current (FIG. 16).

[0078] Although various wirings (the wiring 105, the wiring 1108, the wiring 1105 and the like) are provided in the circuit shown in FIG. 11, these wirings may be connected as long as a normal operation can be performed. For example, the wiring 105 and the wiring 1108 operate at nearly equal potentials, thus, the wirings can be connected to each other to simplify the circuit configuration and reduce the layout area. Furthermore, the wiring 1105 and the wiring 104 may be connected to each other, because the operation is not much influenced by the connection.

[0079] Next, FIG. 18 shows a configuration diagram in which a current is supplied to the load 1101 by using a transistor other than the current source transistor. A gate terminal of the current transistor 1802 is connected to the gate terminal of the current source transistor 102. Thus, the current transistor 1802 can supply a current in accordance with the gate potential of the current source transistor 102. In addition, when the W/L of the current source transistor 102 and the current transistor 1802 is adjusted, the amount of current supplied to the load 1101 can be bought. For example, when the W/L of the current transistor 1802 is small, the amount of current supplied to the load 1101 is reduced, and thereby the amount of Idata can be increased. As a result, writing of current can be carried out quickly. However, when there are varia-

tions in current characteristics of the current source transistor 102 and the current transistor 1802, influences thereof are inevitable.

[0080] In order that the gate-source voltages of the current source transistor 102 and the current transistor 1802 in writing and setting a current are equal to those in outputting a current, a switch 1906 and a wiring 1908 may be connected to each other as shown in FIG. 19. Operations of FIG. 19 are shown in FIGS. 20 and 21. FIG. 20 shows an operation in writing and setting a current whereas FIG. 21 shows an operation in outputting a current. Note that a switch 1902 has a function to prevent an unnecessary current from flowing when a current being written and set, and to prevent incorrect setting. Therefore, in the case where when writing and setting a current, a current flows as shown in FIG. 22 and the setting can be carried out correctly, the switch 1902 may be omitted as shown in FIG. 22.

[0081] It is to be noted that wirings may be connected to each other as long as a normal operation can be performed. Thus, in FIG. 19 and FIG. 22, the wiring 105 may be connected to the wiring 1908.

[0082] FIG. 23 shows a configuration diagram in which a current is supplied to the load 1101 by using another transistor as well as the current source transistor 102. In the case of the current Idata being supplied from the current source circuit 101, when the current leaks to the load 1101 or a current leaks from the load 1101, a proper current cannot be set. The current is controlled by the switch 1102 in the case of FIG. 11, while it is controlled by a multi-transistor 2302 in the case of FIG. 23. A gate terminal of the multi-transistor 2302 is connected to the gate terminal of the current source transistor 102. Therefore, when the switches 1103 and 1104 are on and the current source transistor 102 operates in a saturation region, the multi-transistor 2302 is off. Thus, it does not adversely affect when the current Idata is supplied from the current source circuit 101. On the other hand, when a current is supplied to the load 1101, the current source transistor 102 and the multi-transistor 2302 whose gate terminals are connected to each other operate as a multi-gate transistor. Accordingly, a current smaller than the Idata is supplied to the load 1101. Since the amount of current supplied to the load becomes smaller, the amount of Idata can be increased. As a result, writing of current can be carried out quickly. When there are variations in current characteristics of the current source transistor 102 and the multi-transistor 2302, influences thereof are inevitable. However, a current is supplied to the load 1101 by using also the current source transistor 102, thus influences of the variations can be suppressed.

[0083] FIG. 24 shows a configuration for increasing the current Idata supplied from the current source circuit 101 in a different manner than the one shown in FIG. 18 or 23. In FIG. 24, a parallel transistor 2402 is connected in parallel with the current source transistor 102. Therefore, when a current is supplied from the current source circuit 101, a switch 2401 is turned on. Meanwhile, in the case of a current being supplied to the load 1101, the switch 2401 is turned off. According to this, the current supplied to the load 1101 becomes smaller, and thereby the current Idata supplied from the current source circuit 101 can be increased.

[0084] In that case, however, variations of the parallel transistor 2402 and the current source transistor 102 have an effect. Thus, in the case of FIG. 24, when a current is supplied from the current source circuit 101, the amount of the current may vary. That is, a large current is supplied first and the switch 2401 is turned on in accordance with the current. Then, a current flows into the parallel transistor 2402 and writing of current can be carried out quickly. In other words, this corresponds to a precharge operation. Subsequently, the current supplied from the current source circuit 101 is reduced, and the switch 2401 is turned off. Thus, the current is supplied and written to the current source transistor 102 only. According to this, influences of variations can be prevented. Then, the switch 1102 is turned on and a current is supplied to the load 1101.

[0085] In FIG. 24, the transistor is added in parallel with the current source transistor. FIG. 25 shows a configuration diagram in which a transistor is added in series. In FIG. 25, a series transistor 2502 is connected in series with the current source transistor 102. Therefore, when a current is supplied from the current source circuit 101, a switch 2501 is turned on, and thereby a source and a drain of the series transistor 2002 are short-circuited. When a current is supplied to the load 1101, the switch 2501 is turned off. Thus, the current source transistor 102 and the series transistor 2502 whose gate terminals are connected to each other operate as a multi-gate transistor. Accordingly, the gate length L is increased and the amount of current flowing into the load 1101 is reduced, and thereby the current Idata supplied from the current source circuit 101 can be increased.

[0086] In that case, however, variations of the series transistor 2502 and the current source transistor 102 have an effect. Thus, in the case of FIG. 25, when a current is supplied from the current source circuit 101, the amount of the current may vary. That is, a large current is supplied first and the switch 2501 is turned on in accordance with the current. Then, a current flows only into the current source transistor 102 and writing of current can be carried out quickly. In other words, this corresponds to a precharge operation. Subsequently, the current supplied from the current source circuit 101 is reduced, and the switch 2501 is turned off. Thus, the current is supplied and written to the current source transistor 102 and the series transistor 2502. According to this, influences of variations can be prevented. Then, the switch 1102 is turned on and a current is supplied to the load 1101 by the current source transistor 102 and the series transistor 2502 that constitute a multi-gate transistor.

[0087] It is to be noted that various configurations shown in FIGS. 11 to 25 may be combined to obtain an-

other configuration.

[0088] Although the current source circuit 101 and the load 1101 are switched over in FIGS. 11 to 25, the invention is not limited to this, For example, the current source circuit 101 and a wiring may be switched over. FIG. 26 shows a configuration corresponding to FIG. 11, in which the current source circuit 101 and a wiring are switched over. An operation of FIG. 26 is described hereinafter. First, the current Idata is supplied from the current source circuit 101 to the current source transistor 102, and the switches 1103, 1104 and 1107 are turned on in the case of a current being set. Then, the current source transistor 102 operates as a current source circuit, and the switches 1103, 1104 and 1107 are turned off while switches 2602 and 1102 are turned on in the case of a current being supplied to the load. In this manner, when the switches 1103 and 2602 are turned on/off, the current source circuit 101 and a wiring 2605 are switched over.

[0089] In the case of the current Idata being supplied from the current source circuit 101 to the current source transistor 102, the switch 1102 is turned off and a current is prevented from flowing into the load 1101, though the invention is not limited to this. When the current Idata is supplied from the current source circuit 101 to the current source transistor 102, a current may flow into the load 1101. In that case, the switch 1102 may be omitted.

[0090] The capacitor element 103 holds the gate potential of the current source transistor 102. It is more desirable that the wiring 106 be connected to the source terminal of the current source transistor 102 in order to hold the gate-source voltage.

[0091] Note that FIG. 26 shows a configuration diagram corresponding to FIG. 11, in which the current source circuit 101 and the load 1101 are switched over, though the invention is not limited to this. A configuration in which the current source circuit 101 and the load 1101 are switched over can be achieved in any one of the configurations shown in FIGS. 11 to 25.

[0092] It is to be noted that although the switches are arranged in each part in the configurations described above, the arrangement is not limited to the foregoing. The switches may be disposed anywhere as long as they operate normally.

[0093] In the case of the configuration shown in FIG. 11, for instance, the connection as shown in FIG. 27 may be adopted when the current Idata is supplied from the current source circuit 101 to the current source transistor 102, while the connection as shown in FIG. 28 may be adopted when the current source transistor 102 operates as a current source circuit and a current is supplied to the load 1101. Thus, the configuration shown in FIG. 11 may be connected as shown in FIG. 29. The arrangement of the switches 1102, 1103 and 1104 is modified in FIG. 29, though a normal operation can be performed.

[0094] Similarly, the configuration shown in FIG. 19 may be connected as shown in FIG. 30. The arrangement of the switch 1104 is modified in FIG. 30, though a normal operation can be performed.

[0095] Note that the switches shown in FIG. 11 and the like may be any one of electrical ones and mechanical ones as long as a current flow can be controlled. They may be transistors, diodes, or logic circuits made of combinations thereof. When a transistor being used as a switch, since it operates only as a switch, the polarity (conductivity type) of the transistor is not particularly restricted. However, in the case of an off current being desirable to be small, it is desirable to use a transistor having the polarity less in the off current. As a transistor less in the off current, there is the one in which an LDD region is disposed, and the like. Furthermore, when a transistor functioning as a switch operates in a state where a potential of a source terminal thereof is close to a low potential side power source (Vss, Vgnd, 0 V and the like), an n-channel type is desirably used. On the contrary, when a transistor operates in a state where a potential of the source terminal is close to a high potential side power source (Vdd and the like), a p-channel type is desirably used. The reason for this is that since the absolute value of a gate-source voltage can be made larger, the transistor can efficiently operate as a switch. With both an n-channel type and a p-channel type, a CMOS type switch may be formed.

[0096] Although various examples are shown above, the invention is not limited to this. The current source transistor and various transistors operating as current sources may be disposed in various configurations. In addition, wirings may be connected to each other within a range a normal operation can be performed. Therefore, the invention can be applied to any configuration as long as a similar operation can be performed.

[0097] It is to be noted that this embodiment mode is described with reference to the configurations shown in Embodiment Modes 1 and 2. However, the invention is not limited to this and various changes and modifications are possible unless such changes and modifications depart from the scope of the invention. Therefore, the descriptions in Embodiment Modes 1 and 2 can be applied to this embodiment mode.

(Embodiment Mode 4)

[0098] The configurations each including one current source circuit and one current source transistor are described above. Described in this embodiment mode is the case where a plurality of current source transistors and the like are disposed.

[0099] FIG. 31 shows a configuration corresponding to FIG. 12, in which a plurality of current source transistors are disposed. In FIG. 31, one current source circuit 101 and one operational amplifier 407 are disposed for a plurality of current source transistors 102a and 102b. A plurality of current source circuits or a plurality of operational amplifiers may be disposed for a plurality of current source transistors. However, since the circuit area increases, one current source circuit 101 and one operational amplifier 407 are preferably disposed. Though,

the amplifier circuit (source follower circuit 907) in FIG. 9 is constituted by two transistors in many cases, thus, a plurality of amplifier circuits (source follower circuits) may be disposed for a plurality of current source transistors.

[0100] A configuration of FIG. 31 is described next. First, the current source circuit 101 and the operational amplifier 407 are disposed, which are collectively called a resource circuit 3101 hereinafter. The resource circuit 3101 is connected to a current line 3102 connected to the current source circuit 101 and a voltage line 3103 connected to an output terminal of the operational amplifier 407. The current line 3102 and the voltage line 3103 are connected to a plurality of unit circuits 3104a and 3104b. The unit circuit 3104a includes the current source transistor 102a, a capacitor element 103a, switches 1102a, 1103a, 1104a, 1106a, and 1107a, and the like. The unit circuit 3104a is connected to a load 1101a connected to a wiring 1105a. The unit circuit 3104b has a similar configuration to the unit circuit 3104a. The two unit circuits are connected herein for simplicity, though the invention is not limited to this. The number of unit circuits may be determined arbitrarily.

[0101] As for operations, since a plurality of unit circuits are connected to one current line 3102 and one voltage line 3103, each unit circuit is selected and a current and a voltage are sequentially supplied thereto from the resource circuit 3101 through the current line 3102 and the voltage line 3103. For example, the operation is carried out such that the switches 1103a, 1104a and 1107a are turned on first to input a current and a voltage to the unit circuit 3104a, and switches 1103b, 1104b and 1107b are turned on next to input a current and a voltage to the unit circuit 3104b.

[0102] These switches can be controlled by a digital circuit such as a shift register, a decoder circuit, a counter circuit, and a latch circuit.

[0103] In the case where the loads 1101a, 1101b and the like are display elements such as EL elements, the unit circuit and the load constitute one pixel, and the resource circuit 3101 corresponds to (a part of) a signal line driver circuit that supplies a signal to a pixel connected to a signal line (current line 3102 and voltage line 3103). In other words, FIG. 31 shows one column of pixels and (a part of) a signal line driver circuit. In that case, a current output from the current source circuit 101 corresponds to an image signal. When this image signal current is changed in an analog manner or a digital manner, the proper amount of current can be supplied to each of the loads 1101a and 1101b (display element such as EL element). At this time, the switches 1103a, 1104a and 1107a, the switches 1103b, 1104b and 1107b, and the like are controlled by a gate line driver circuit.

[0104] Further, in the case of the current source circuit 101 in FIG. 31 being (a part of) a signal line driver circuit, the current source circuit 101 is required to output a current accurately without being influenced by variations in current characteristics and size of transistors. Accordingly, the current source circuit 101 in (a part of) the signal line driver circuit is constituted by a circuit including a transistor that functions similarly to the current source transistors 102, 202, 302, and 10002, and a current can be supplied from another current source circuit to the current source transistor in (a part of) the signal line driver circuit. In other words, when the loads 1101a, 1101b and the like in FIG. 31 are a signal line, a pixel connected to the signal line, and the like, the unit circuits 3104a and 3104b constitute (a part of) the signal line driver circuit, and the resource circuit 3101 is (a part of) a current source circuit that supplies a signal to a current source transistor (current source circuit) in the signal line driver circuit connected to the current line 3102. That is, FIG. 31 shows a plurality of signal lines, (a part of) a signal line driver circuit, and (a part of) a current source circuit that supplies a current to the signal line driver circuit.

[0105] In such a case, a current output from the current source circuit 101 corresponds to a current supplied to a signal line and a pixel. Therefore, in the case of, for instance, a current corresponding to a current output from the current source circuit 101 being supplied to a signal line and a pixel connected to the signal line, the current output from the current source circuit 101 corresponds to an image signal. When this image signal current is changed in an analog manner or a digital manner, the proper amount of current can be supplied to each load (a signal line and a pixel connected to the signal line). At this time, the switches 1103a, 1104a and 1107a, the switches 1103b, 1104b and 1107b, and the like are controlled by a circuit (shift register, latch circuit and the like) that is a part of the signal line driver circuit.

[0106] It is to be noted that the circuit or the like (shift register, latch circuit or the like) for controlling the switches 1103a, 1104a and 1107a and the switches 1103b, 1104b and 1107b is disclosed in International Publication WO 03/038796, International Publication WO 03/038797, and the like. The invention can be implemented in combination with the descriptions thereof.

[0107] Alternatively, in the case of a predetermined amount of current being output from the current source circuit 101, a switch or the like being used for controlling whether to supply the current, and a current corresponding thereto being supplied to a signal line and a pixel, the current output from the current source circuit 101 corresponds to a signal current for supplying a predetermined amount of current. The switch for determining whether to supply a current to a signal line and a pixel is controlled in a digital manner to control the amount of current supplied to the signal line and the pixel, and thereby the proper amount of current can be supplied to each load (signal line and pixel). In that case, the switches 1103a, 1104a and 1107a, the switches 1103b, 1104b and 1107b, and the like are controlled by a circuit (shift register, latch circuit or the like) that is a part of a signal line driver circuit. At this time, however, a driver circuit (shift register, latch circuit or the like) is needed for controlling the switch that determines whether to supply a current to a signal line

and a pixel. Accordingly, the driver circuit (shift register, latch circuit or the like) for controlling the switch is required as well as a driver circuit (shift register, latch circuit or the like) for controlling the switches 1103a, 1104a and 1107a, the switches 1103b, 1104b and 1107b, and the like. These driver circuits may be provided separately. For example, a shift register for controlling the switches 1103a, 1104a and 1107a, and the switches 1103b, 1104b and 1107b may be provided independently. Instead, the driver circuit (shift register, latch circuit or the like) for controlling the switch and the driver circuit (shift register, latch circuit or the like) for controlling the switches 1103a, 1104a and 1107a, the switches 1103b, 1104b and 1107b, and the like may be shared partially or entirely. For instance, one shift register may be used for controlling both the switches, or an output (image signal) of a latch circuit and the like may be used in a driver circuit (shift register, latch circuit or the like) for controlling the switch that determines whether to supply a current to a signal line and a pixel.

[0108] It is to be noted that the driver circuit (shift register, latch circuit or the like) for controlling the switch that determines whether to supply a current to a signal line and a pixel and the driver circuit (shift register, latch circuit or the like) for controlling the switches 1103a, 1104a and 1107a, the switches 1103b, 1104b and 1107b, and the like are disclosed in International Publication WO 03/038793, International Publication WO 03/038794, International Publication WO 03/038795 and the like. The invention can be implemented in combination with the descriptions thereof.

[0109] FIG. 31 shows the case in which the current source transistors 102a and 102b are disposed for the loads 1101a and 1101b respectively. Next, the case in which a plurality of current source transistors are disposed for one load is shown in FIG. 32. Two unit circuits are connected to one load herein for simplicity, though the invention is not limited to this. Three or more unit circuits may be connected or a single unit circuit may be connected. The amount of current flowing into a load 1101aa can be controlled by turning on/off a switch 3201aa and a switch 3201ba. In the case of, for instance, a current value (Iaa) output from a unit circuit 3104aa being different from a current value (Iba) output from a unit circuit 3104ba, four different amounts of current flowing into the load 1101aa can be controlled by turning on/off each the switch 3201aa and the switch 3201ba. For example, when Iba = 2*Iaa is satisfied, the amount of current can be controlled by two bits. Therefore, in the case where the switch 3201aa and the switch 3201ba are turned on/off by digital data corresponding to each bit, a digital to analog conversion can be achieved by using the configuration shown in FIG. 32. Thus, in the case of the loads 1101aa and 1101bb being signal lines, (a part of) a signal line driver circuit can be obtained by using the configuration shown in FIG. 32. In this case, a digital image signal can be converted into an analog image signal current. The switch 3201aa and the switch 3201ba can be turned on/off by an image signal. Accordingly, the switch 3201aa and the switch 3201ba can be controlled by a circuit (latch circuit) and the like for outputting an image signal.

[0110] The switch 3201aa and the switch 3201ba may be turned on/off over time. For example, in a certain period, the switch 3201aa is turned on while the switch 3201ba is turned off, a current is set so as to be input from a resource circuit 3101b to the unit circuit 3104ba and output with accuracy, and a current is supplied from the unit circuit 3104aa to the load 1101aa. In another period, the switch 3201aa is turned off while the switch 3201ba is turned on, a current is set so as to be input from a resource circuit 3101a to the unit circuit 3104aa and output with accuracy, and a current is supplied from the unit circuit 3104ba to the load 1101aa. In this manner, the switches may be operated by switching over time.

[0111] In FIG. 32, the two resource circuits 3101a and 3101b are used for supplying a current to the unit circuits 3104aa, 3104ba, 3104ab, and 3104bb. FIG. 33 shows the case in which the one resource circuit 3101 is used for supplying a current to unit circuits 3104ca, 3104cb, 3104da, and 3104db.

[0112] It is supposed that, for example, in the case of a wiring 3304c being an H signal, switches 3301ca, 3302ca and 3303cb are turned on while switches 3303ca, 3301cb and 3302cb are turned off. Then, the unit circuit 3104ca becomes capable of being supplied with a current from the resource circuit 3101 whereas the unit circuit 3104cb becomes capable of supplying a current to a load 1101ca. On the contrary, in the case of the wiring 3304c being an L signal, the unit circuit 3104cb becomes capable of being supplied with a current from the resource circuit 3101 whereas the unit circuit 3104ca becomes capable of supplying a current to the load 1101ca. Further, the wiring 3304c, a wiring 3304d and the like may be selected in sequence by a signal. In this manner, the operation of a unit circuit may be switched over time.

[0113] In the case of the loads 1101ca and 1101da being signal lines, (a part of) a signal line driver circuit can be obtained by using the configuration shown in FIG. 33. In addition, the wiring 3304c, the wiring 3304d and the like may be controlled by a shift register and the like.

[0114] Although in this embodiment mode, the configuration including a plurality of current source transistors is shown with reference to the configuration in FIG. 12, the invention is not limited to this. The similar configuration can be achieved with reference to another configuration than the one shown in FIG. 12.

[0115] It is to be noted that this embodiment mode is described with reference to the configurations shown in Embodiment Modes 1, 2 and 3. However, the invention is not limited to this and various changes and modifications are possible unless such changes and modifications depart from the scope of the invention. Therefore, the descriptions in Embodiment Modes 1, 2 and 3 can be applied to this embodiment mode.

(Embodiment Mode 5)

[0116] Described in this embodiment mode is the case in which the invention is applied to a pixel including a display element.

[0117] Although this embodiment mode will be described with reference to the configurations shown in FIG. 1 (FIGS. 11, 2 and 5) and FIG. 3 (FIG. 8), the invention is not limited to this. This embodiment mode can be applied to the various configurations shown in Embodiment Modes 1 to 4.

[0118] FIGS. 34 and 35 each shows a configuration in which the current source circuit 201 supplies a signal current as an image signal. The direction of current flow is the same in FIG. 34 and FIG. 35, though the polarity of the current source transistor 202 is different. Therefore, the connection is different between in FIG. 34 and FIG. 35. Note that an EL element is taken as an example of the load 1101 herein.

[0119] When a signal current supplied as an image signal by the current source circuit 201 is an analog value, images can be displayed with analog gray scale. When a signal current is a digital value, images can be displayed with digital gray scale. In order to achieve multi-level gray scale, digital gray scale may be combined with a time gray scale method or an area gray scale method.

[0120] It is to be noted that the time gray scale method is not described in no more details herein, and it may be carried out in accordance with Japanese Patent Application No. 2001-5426, Japanese Patent Application No. 2001-343933 and the like.

[0121] One gate line is shared to control each of the switches 1102, 1104, 1106, and 1107 by adjusting the polarity of transistors. According to this, the aperture ratio can be improved, though respective gate lines may be disposed. In particular, when adopting the time gray scale method, a period in which a current is not supplied to the load 1101 (EL element) is needed. In that case, another wiring may be provided as a gate line for controlling the switch 1102 that can stop supplying a current to the load 1101 (EL element).

[0122] FIG. 36 shows a configuration of a pixel including a sub-current source circuit 3601, in which images are displayed in accordance with whether a current supplied by the sub-current source circuit 3601 flows or not. When a selective gate line 3606 being selected, a switch 3604 is turned on and a digital image signal (a voltage value in general) is input from a signal line 3605 to a capacitor element 3603. It is to be noted that the capacitor element 3603 can be omitted when gate capacitance of a transistor is used instead. A switch 3602 is turned on/off by the stored digital image signal. The switch 3602 controls whether a current supplied by the current source circuit 3601 flows to the load 1101 or not. As a result, images can be displayed.

[0123] In order to achieve multi-level gray scale, the time gray scale method and the area gray scale method may be adopted in combination.

[0124] Although only the one sub-current source circuit 3601 and the one switch 3602 are disposed in FIG. 36, the invention is not limited to this. A plurality of pairs of current source circuit and switch may be disposed to control whether a current from each current source circuit flows or not, and the sum of the current may flow to the load 1101.

[0125] Next, a specific configuration example of FIG. 36 is shown in FIG. 37. The configuration shown in FIG. 1 (FIG. 11, FIG. 2 and FIG. 5) is adopted herein for a current source transistor. A current is supplied from the current source circuit 201 to the current source transistor 202 and the capacitor element 3603, and the gate terminal of the current source transistor 202 is set to a proper voltage. Then, the switch 3602 is turned on/off in accordance with an image signal input from the signal line 3605 to supply a current to the load 1101, and thereby images are displayed.

[0126] It is to be noted that this embodiment mode is described with reference to the configurations shown in Embodiment Modes 1 to 4. However, the invention is not limited to this and various changes and modifications are possible unless such changes and modifications depart from the scope of the invention. Therefore, the descriptions in Embodiment Modes 1 to 4 can be applied to this embodiment mode.

(Embodiment Mode 6)

[0127] Described in this embodiment mode are configurations and operations of a display device, a signal line driver circuit and the like. The circuit of the invention can be applied to a part of a signal line driver circuit and a pixel.

[0128] A display device comprises, as shown in FIG. 38, a pixel array 3801, a gate line driver circuit 3802 and a signal line driver circuit 3810. The gate line driver circuit 3802 sequentially outputs a selective signal to the pixel array 3801. The signal line driver circuit 3810 sequentially outputs a video signal to the pixel array 3801. In the pixel array 3801, a state of light is controlled depending on a video signal to display images. A video signal input from the signal line driver circuit 3810 to the pixel array 3801 is a current in many cases. In other words, a state of a display element and an element for controlling the display element that are disposed in each pixel changes in accordance with a video signal (current) input from the signal line driver circuit 3810. As a display element disposed in each pixel, an EL element, an element used for FED (Field Emission Display) and the like are taken as an example.

[0129] It is to be noted that a plurality of gate line driver circuits 3802 may be disposed as well as a plurality of signal line driver circuits 3810.

[0130] The signal line driver circuit 3810 can be divided into plural parts. It can be roughly divided, for instance, into a shift register 3803, a first latch circuit (LAT1) 3804, a second latch circuit (LAT2) 3805, and a digital to analog

converter circuit 3806. The digital to analog converter circuit 3806 may have a function to convert a voltage to a current as well as a function to perform gamma correction. That is, the digital to analog converter circuit 3806 has a circuit for outputting a current (video signal) to a pixel, namely a current source circuit, to which the invention can be applied.

[0131] As shown in FIG. 36, depending on a pixel configuration, a digital voltage signal for a video signal and a controlling current for a current source circuit in a pixel are input to the pixel in some cases. In that case, the digital to analog converter circuit 3806 does not have a digital to analog conversion function but has a function to convert a voltage to a current, and has a circuit for outputting the current to a pixel as a controlling current, namely a current source circuit to which the invention can be applied.

[0132] Furthermore, a pixel includes a display element such as an EL element, and a circuit for outputting a current (video signal) to the display element, namely a current source circuit to which the invention can be applied.

[0133] An operation of the signal line driver circuit 3810 is briefly described. The shift register 3803 is constituted by a plurality of columns of flip flop circuits (FF) and the like, to which a clock signal (S-CLK), a start pulse (SP) and an inverted clock signal (S-CLKb) are input. In accordance with the timing of these signals, a sampling pulse is output in sequence.

[0134] The sampling pulse output from the shift register 3803 is input to the first latch circuit (LAT1) 3804. In accordance with the timing of the sampling pulse, the first latch circuit (LAT1) 3804 holds a video signal in each column, which has been input from a video signal line 3808. It is to be noted that in the case of the digital to analog converter circuit 3806 being disposed, the video signal is a digital value. The video signal at this time is a voltage in many cases.

[0135] In the case of the first latch circuit 3804 and the second latch circuit 3805 being circuits capable of holding an analog value, the digital to analog converter circuit 3806 can be omitted in many cases. In that case, the video signal may be a current. Further, in the case of data output to the pixel array 3801 being binary data, that is, a digital value, the digital to analog converter circuit 3806 can be omitted in many cases.

[0136] When the holding of video signals is completed until the last column in the first latch circuit (LAT1) 3804, a latch pulse (Latch Pulse) is input from a latch control line 3809 during a horizontal flyback period, and the video signals held in the first latch circuit (LAT1) 3804 are transferred to the second latch circuit (LAT2) 3805 at a time. Then, the video signals held in the second latch circuit (LAT2) 3805 are input to the digital to analog converter circuit 3806 per each row. Signals output from the digital to analog converter circuit 3806 are input to the pixel array 3801.

[0137] During a period in which the video signals held in the second latch circuit (LAT2) 3805 are input to the digital to analog converter circuit 3806 and then to the pixel 3801, the shift register 3803 outputs a sampling pulse newly. That is, the two operations are carried out at the same time. According to this, a line sequential driving becomes possible. These operations are repeated thereafter.

[0138] In the case of a current source circuit included in the digital to analog converter circuit 3806 being a circuit that performs a set operation and an output operation, that is, a circuit to which a current is input from another current source circuit and which is capable of outputting a current without being influenced by variations in characteristics of transistors, a circuit for supplying a current to the current source circuit is required. In that case, a reference current source circuit 3814 . is disposed.

[0139] Note that configurations of the signal line driver circuit and the like are not limited to the ones shown in FIG. 38.

[0140] For example, in the case of the first latch circuit 3804 and the second latch circuit 3805 being circuits capable of holding an analog value, as shown in FIG. 39, a video signal (analog current) may be input from the reference current source circuit 3814 to the first latch circuit (LAT1) 3804. Further, in FIG. 39, the second latch circuit 3805 is omitted in some cases. In that case, the first latch circuit 3804 often includes more current source circuits.

[0141] In such a case, the invention can be applied to a current source circuit in the digital to analog converter circuit 3806 shown in FIG. 38. The digital to analog converter circuit 3806 comprises a lot of unit circuits, and the reference current source circuit 3814 includes the current source circuit 101 and the amplifier circuit 107.

[0142] The invention can also be applied to a current source circuit in the first latch circuit (LAT1) 3804 shown in FIG. 39. The first latch circuit (LAT1) 3804 comprises a lot of unit circuits, and the reference current source circuit 3814 includes the current source circuit 101.

[0143] Furthermore, the invention can be applied to a pixel (current source circuit included therein) in the pixel array 3801 shown in FIG. 38 and FIG. 39. The pixel array 3801 comprises a lot of unit circuits, and the signal line driver circuit 3810 includes the current source circuit 101 and the amplifier circuit 107.

[0144] That is, circuits each for supplying a current are disposed throughout a circuit. Such current source circuit is required to output a current with accuracy. Therefore, another current source circuit is used for setting a transistor to output a current with accuracy. The another current source circuit is also required to output a current with accuracy. Thus, as shown in FIGS. 40 to 42, a basic current source circuit is disposed in a certain area, then current source transistors are set in sequence. According to this, a current source circuit can output a current with accuracy, to which the invention can be applied.

[0145] As set forth above, any type of transistor may

be used for the transistor in the invention and the transistor may be formed on any type of substrate. Accordingly, the circuits shown in FIG. 38, FIG. 39 and the like may be formed entirely on a glass substrate, a plastic substrate, a single crystalline substrate, an SOI substrate or other substrates. Alternatively, a part of the circuits shown in FIG. 38, FIG. 39 and the like may be formed on a substrate, and the other part of the circuits shown in FIG. 38, FIG. 39 and the like may be formed on another substrate. In other words, not all the circuits shown in FIG. 38, FIG. 39 and the like are required to be formed on the same substrate. In FIG. 38, FIG. 39 and the like, for example, the pixel 3801 and the gate line driver circuit 3802 may be formed on a glass substrate by using TFTs, the signal line driver circuit 3810 (or a part of the same) may be formed on a single crystalline substrate, and an IC chip thereof may be connected by COG (Chip On Glass) to be disposed on the glass substrate. Alternatively, the IC chip may be connected to the glass substrate by TAB (Tape Auto Bonding) or by using a printed substrate.

[0146] It is to be noted that this embodiment mode is described with reference to the configurations shown in Embodiment Modes 1 to 5. Therefore, the descriptions in Embodiment Modes 1 to 5 can be applied to this embodiment mode.

(Embodiment Mode 7)

[0147] The invention can be applied to an electronic circuit constituting a display portion of an electronic appliance. Such an electronic appliance includes a video camera, a digital camera, a goggle type display (head mounted display), a navigation system, an audio reproducing device (an in-car audio system, an audio component set, and the like), a laptop personal computer, a game player, a portable information terminal (a mobile computer, a mobile phone, a portable game player, an electronic book, and the like), an image reproducing device provided with a recording medium (specifically, a device that reproduces a recording medium such as a Digital Versatile Disc (DVD) and includes a display capable of displaying the reproduced images), and the like. That is, the invention can be applied to an electronic circuit constituting a display portion of these appliances (for instance, a pixel, a signal line driver circuit for driving the pixel, and the like). Specific examples of these electronic appliances are shown in FIGS. 43A to 43H.

[0148] FIG. 43A shows a light emitting device (the light emitting device means here a display device using a self-luminous type light emitting element for a display portion) that includes a housing 13001, a supporting base 13002, a display portion 13003, speaker portions 13004, a video input terminal 13005, and the like. The invention can be applied to an electronic circuit that constitutes the display portion 13003. Further, according to the invention, the light emitting device shown in FIG. 43A is completed. Since the light emitting device is a self-luminous type, it requires no backlight, and thereby the display portion thereof can be made thinner than a liquid crystal display Note that the light emitting device refers to all display devices for displaying information, including ones for personal computers, for TV broadcasting reception, for advertisement and the like.

[0149] FIG. 43B shows a digital still camera that includes a main body 13101, a display portion 13102, an image receiving portion 13103, operating keys 13104, an external connecting port 13105, a shutter 13106, and the like. The invention can be applied to an electronic circuit that constitutes the display portion 13102. Further, according to the invention, the digital still camera shown in FIG. 43B is completed.

[0150] FIG. 43C shows a laptop personal computer that includes a main body 13201, a housing 13202, a display portion 13203, a keyboard 13204, an external connecting port 13205, a pointing mouse 13206, and the like. The invention can be applied to an electronic circuit that constitutes the display portion 13203. Further, according to the invention, the light emitting device shown in FIG. 43C is completed.

[0151] FIG. 43D shows a mobile computer that includes a main body 13301, a display portion 13302, a switch 13303, operating keys 13304, an infrared port 13305, and the like. The invention can be applied to an electronic circuit that constitutes the display portion 13302. Further, according to the invention, the mobile computer shown in FIG. 43D is completed.

[0152] FIG. 43E shows a portable image reproducing device provided with a recording medium (specifically a DVD reproducing device), that includes a main body 13401, a housing 13402, a display portion A13403, a display portion B13404, a recording medium (such as a DVD) reading portion 13405, an operating key 13406, a speaker portion 13407, and the like. The display portion A13403 mainly displays image data whereas the display portion B13404 mainly displays character data. The invention can be applied to an electronic circuit that constitutes the display portions A13403 and B13404. It is to be noted that the image reproducing device provided with a recording medium includes a home game player and the like. Further, according to the invention, the DVD reproducing device shown in FIG. 43E is completed.

[0153] FIG. 43F shows a goggle type display (head mounted display) that includes a main body 13501, a display portion 13502, and an arm portion 13503. The invention can be applied to an electronic circuit that constitutes the display portion 13502. Further, according to the invention, the goggle type display shown in FIG. 43F is completed.

[0154] FIG. 43G shows a video camera that includes a main body 13601, a display portion 13602, a housing 13603, an external connecting port 13604, a remote control receiving portion 13605, an image receiving portion 13606, a battery 13607, an audio input portion 13608, operating keys 13609, and the like. The invention can be applied to an electronic circuit that constitutes the display

portion 13602. Further, according to the invention, the video camera shown in FIG. 43G is completed.

[0155] FIG. 43H shows a mobile phone that includes a main body 13701, a housing 13702, a display portion 13703, an audio input portion 13704, an audio output portion 13705, an operating key 13706, an external connecting port 13707, an antenna 13708, and the like. The invention can be applied to an electronic circuit that constitutes the display portion 13703. It is to be noted that current consumption of the mobile phone can be suppressed when the display portion 13703 displays white characters on a black background. Further, according to the invention, the mobile phone shown in FIG. 43H is completed.

[0156] When the luminance of the light emitting material is improved in the future, it can be used for a front type or rear type projector by magnifying and projecting light including output image data by a lens and the like.

[0157] The aforementioned electronic appliances are becoming to be more used for displaying data distributed through a telecommunication path such as Internet and a CATV (Cable Television System), and in particular used for displaying moving pictures data. A light emitting device is suitable for displaying moving pictures because a light emitting material can exhibit a remarkably high response.

[0158] Furthermore, since light emitting parts consume power in a light emitting device, data is desirably displayed so that the light emitting parts may occupy as an area small as possible. Accordingly, in the case of a light emitting device being used for a display portion that mainly displays character data, such as the one of a portable information terminal, particularly the one of a mobile phone or an audio reproducing device, it is preferably operated so that the character data emits light by using non-light emitting parts as background.

[0159] As set forth above, the application range of the invention is so wide that it can be applied to electronic appliances of all fields. In addition, the electronic appliances shown in this embodiment mode may include a semiconductor device with any one of the configurations shown in Embodiment Modes 1 to 4.

Claims

1. A semiconductor device comprising:

   a circuit for controlling a current supplied to a load by a transistor a source or a drain of which is connected to a current source circuit; and
   an amplifier circuit for controlling a source potential or a drain potential of the transistor so that the transistor operates in a saturation region when a current is supplied from the current source circuit to the transistor.

2. A semiconductor device comprising:

   a circuit for controlling a current supplied to a load by a transistor a source or a drain of which is connected to a current source circuit; and
   an amplifier circuit for stabilizing a source potential or a drain potential of the transistor.

3. A semiconductor device comprising:

   a circuit for controlling a current supplied to a load by a transistor a source or a drain of which is connected to a current source circuit; and
   a feedback circuit for stabilizing a source potential or a drain potential of the transistor.

4. A semiconductor device comprising:

   a transistor for controlling a current supplied to a load; and
   an operational amplifier,
   wherein an inverting input terminal of the operational amplifier is connected to a drain terminal side of the transistor connected to a current source circuit;
   a non-inverting input terminal of the operational amplifier is connected to a gate terminal side of the transistor; and
   an output terminal of the operational amplifier is connected to a source terminal side of the transistor.

5. A semiconductor device comprising:

   a transistor for controlling a current supplied to a load; and
   an operational amplifier,
   wherein an inverting input terminal of the operational amplifier is connected to a drain terminal side of the transistor connected to a current source circuit;
   a non-inverting input terminal of the operational amplifier is connected to a gate terminal side of the transistor; and
   an output terminal of the operational amplifier is connected to the drain terminal side of the transistor.

6. A semiconductor device comprising:

   a transistor for controlling a current supplied to a load; and
   a voltage follower circuit,
   wherein an input terminal of the voltage follower circuit is connected to a gate terminal side of the transistor connected to a current source circuit; and
   an output terminal of the voltage follower circuit is connected to a drain terminal side of the transistor.

7. The semiconductor device according to claim 6, wherein the voltage follower circuit is constituted by a source follower circuit.

8. A light emitting device comprising a display portion using the semiconductor device according to any one of claims 1 to 6.

9. A digital still camera comprising a display portion using the semiconductor device according to any one of claims 1 to 6.

10. A laptop personal computer comprising a display portion using the semiconductor device according to any one of claims 1 to 6.

11. A mobile computer comprising a display portion using the semiconductor device according to any one of claims 1 to 6.

12. An image reproducing device comprising a display portion using the semiconductor device according to any one of claims 1 to 6.

13. A goggle type display comprising a display portion using the semiconductor device according to any one of claims 1 to 6.

14. A video camera comprising a display portion using the semiconductor device according to any one of claims 1 to 6.

15. A mobile phone comprising a display portion using the semiconductor device according to any one of claims 1 to 6.

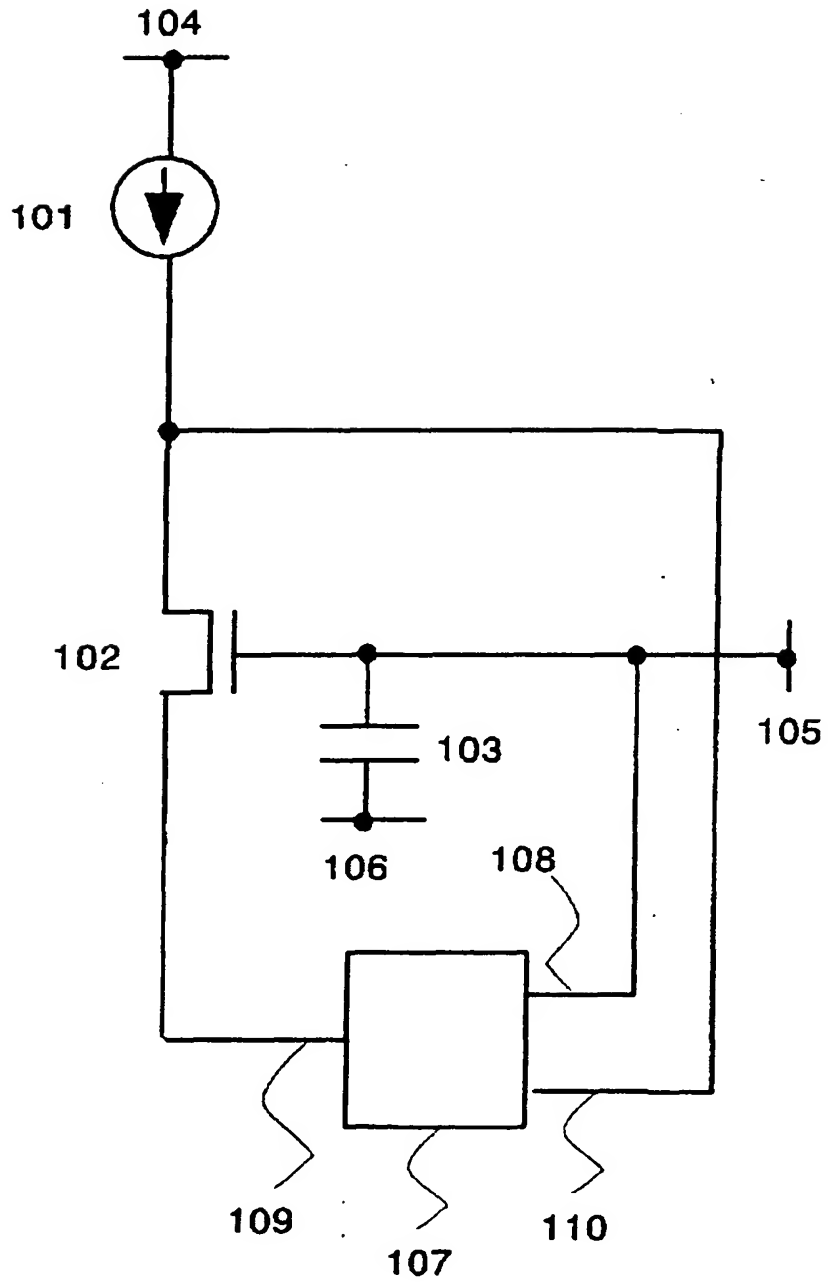


FIG. 1

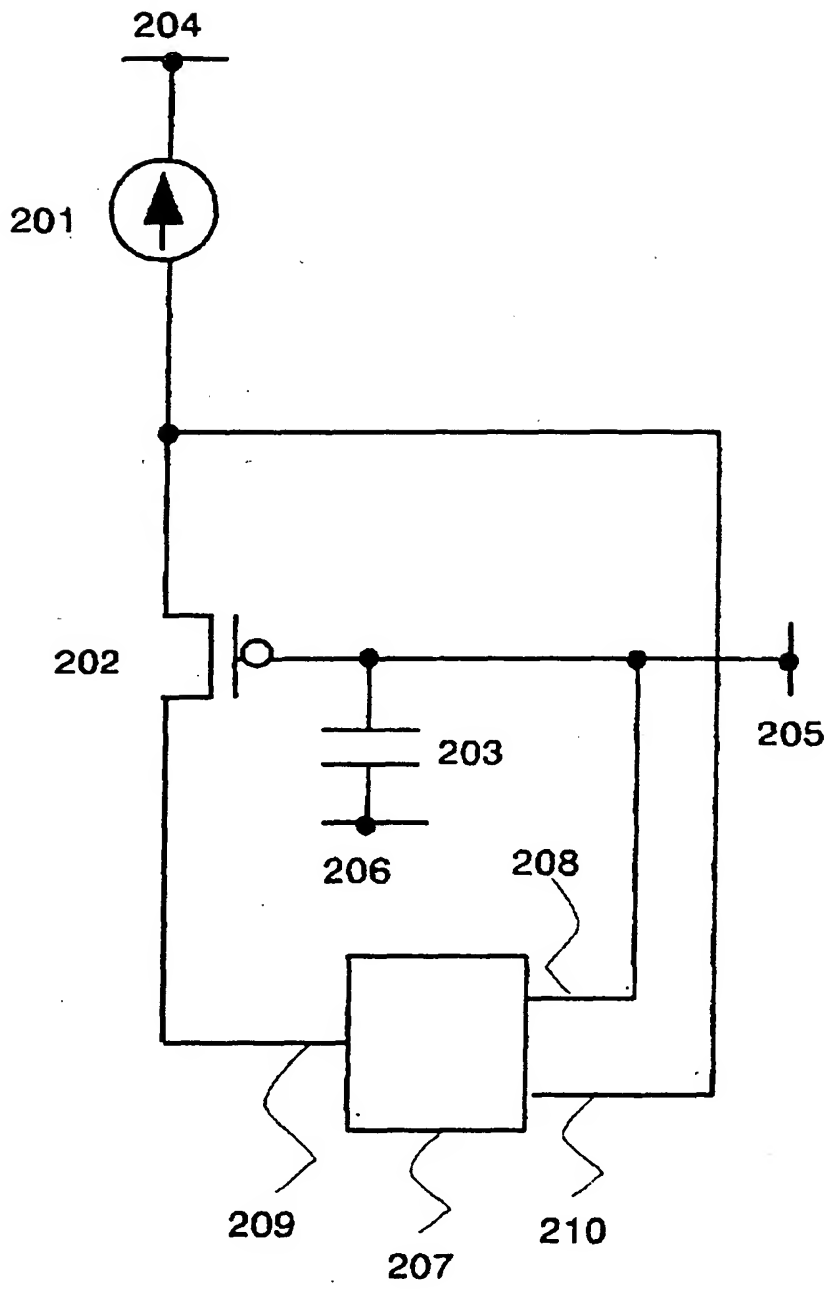


FIG. 2

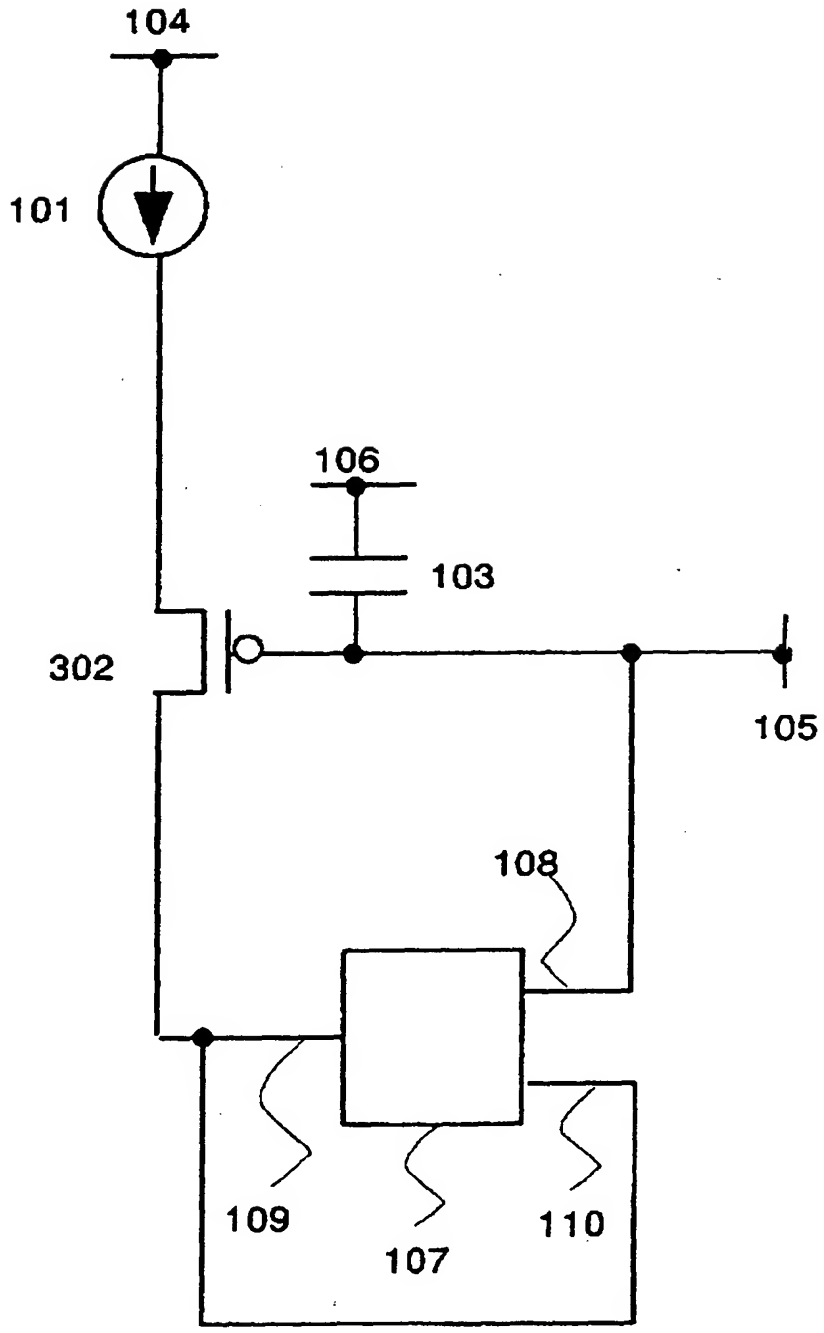


FIG. 3

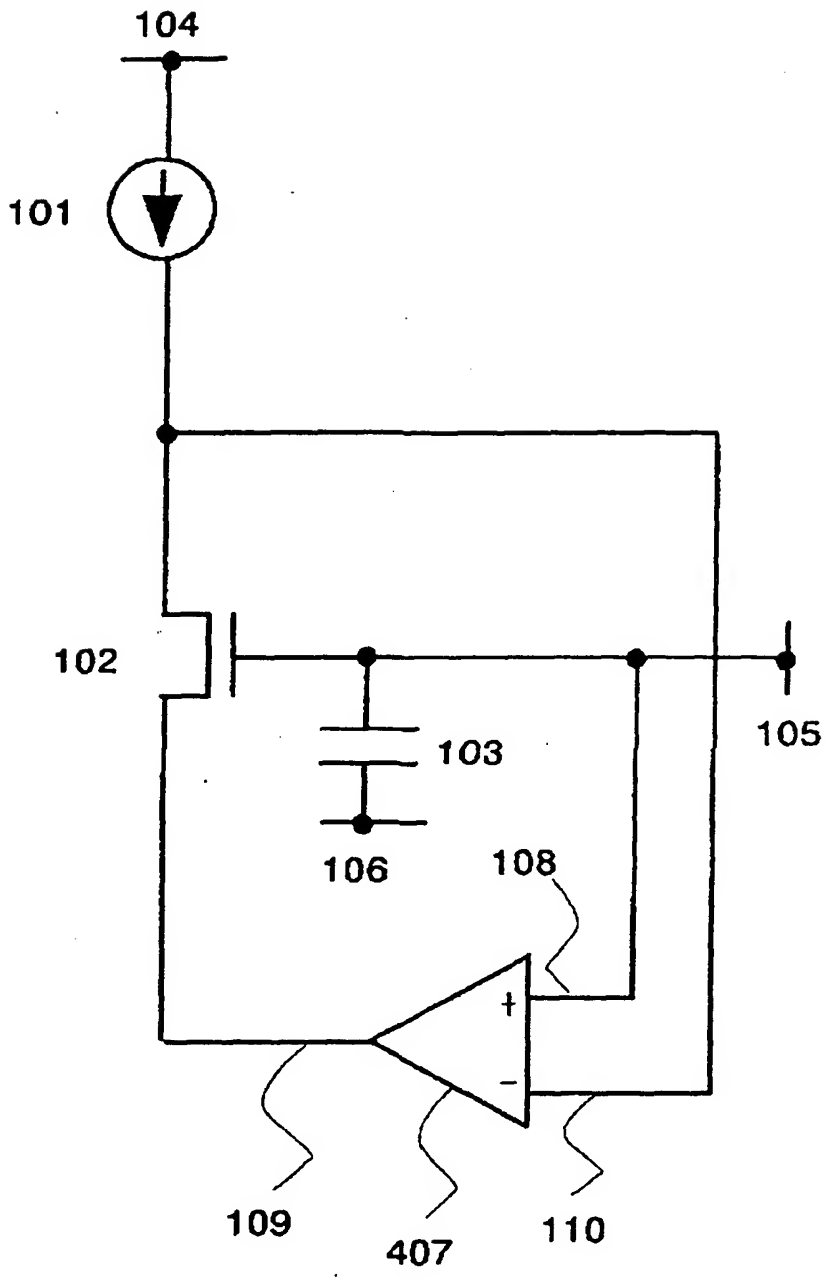


FIG. 4

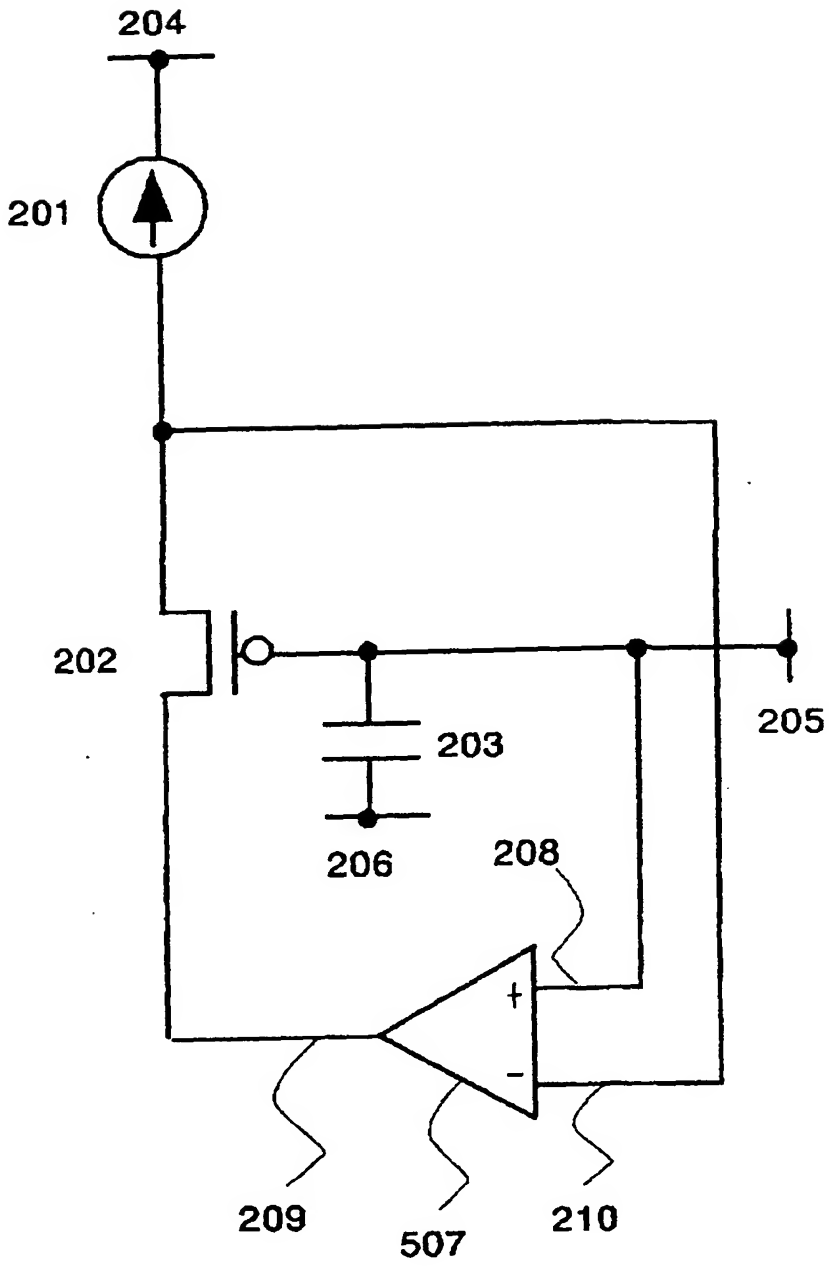


FIG. 5

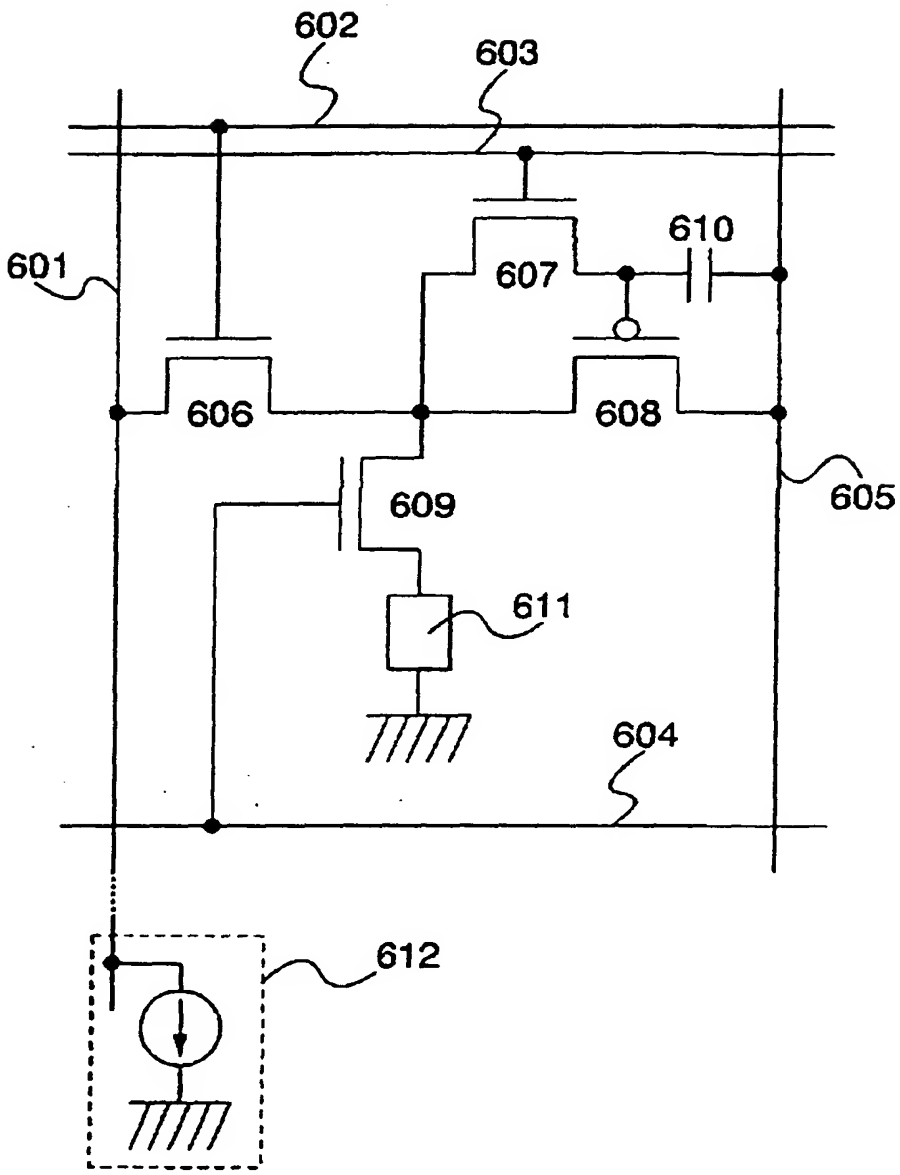


FIG. 6

during signal inputting

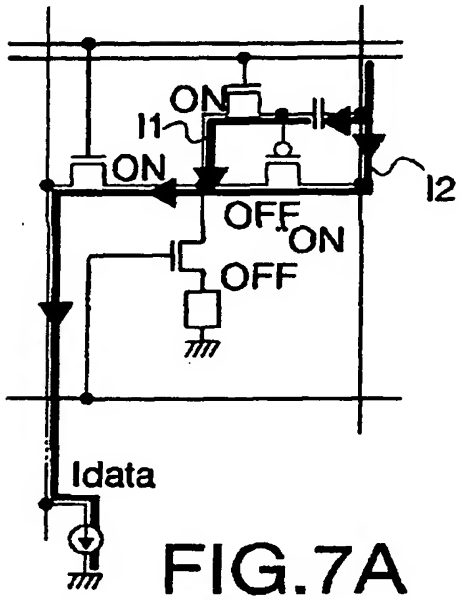


FIG.7A

when signal inputting is completed

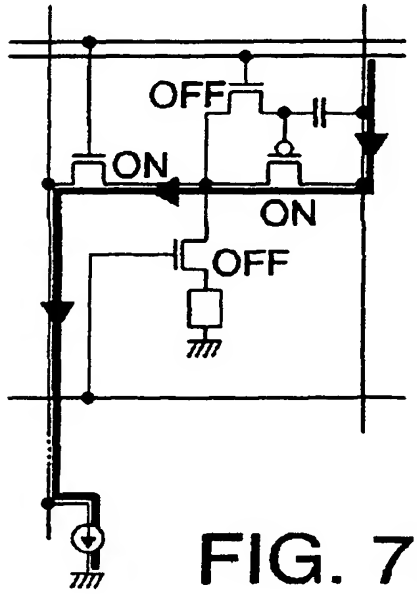


FIG. 7B

during light emission

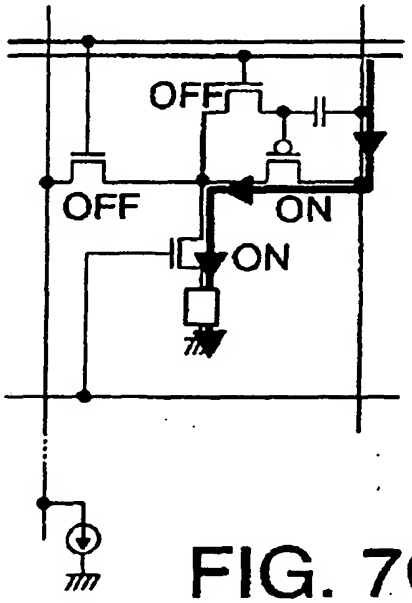


FIG. 7C

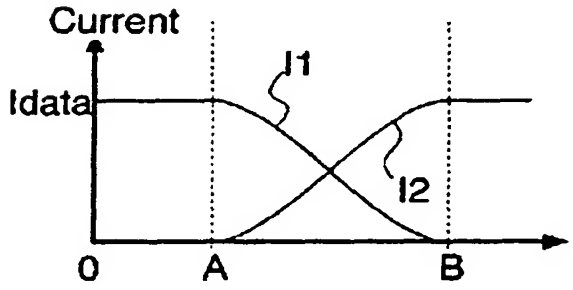


FIG. 7D

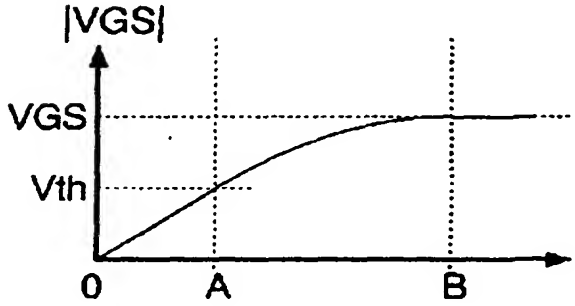


FIG. 7E

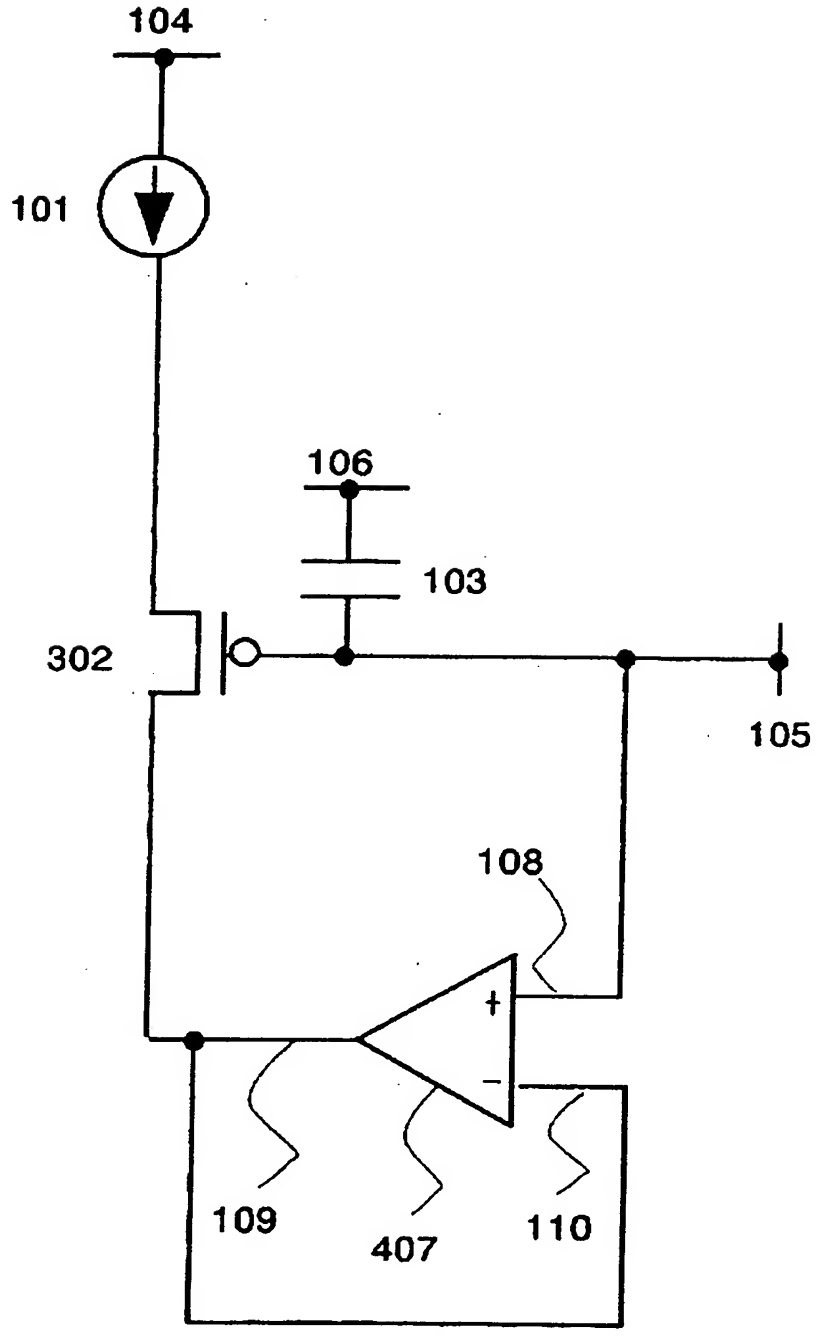


FIG. 8

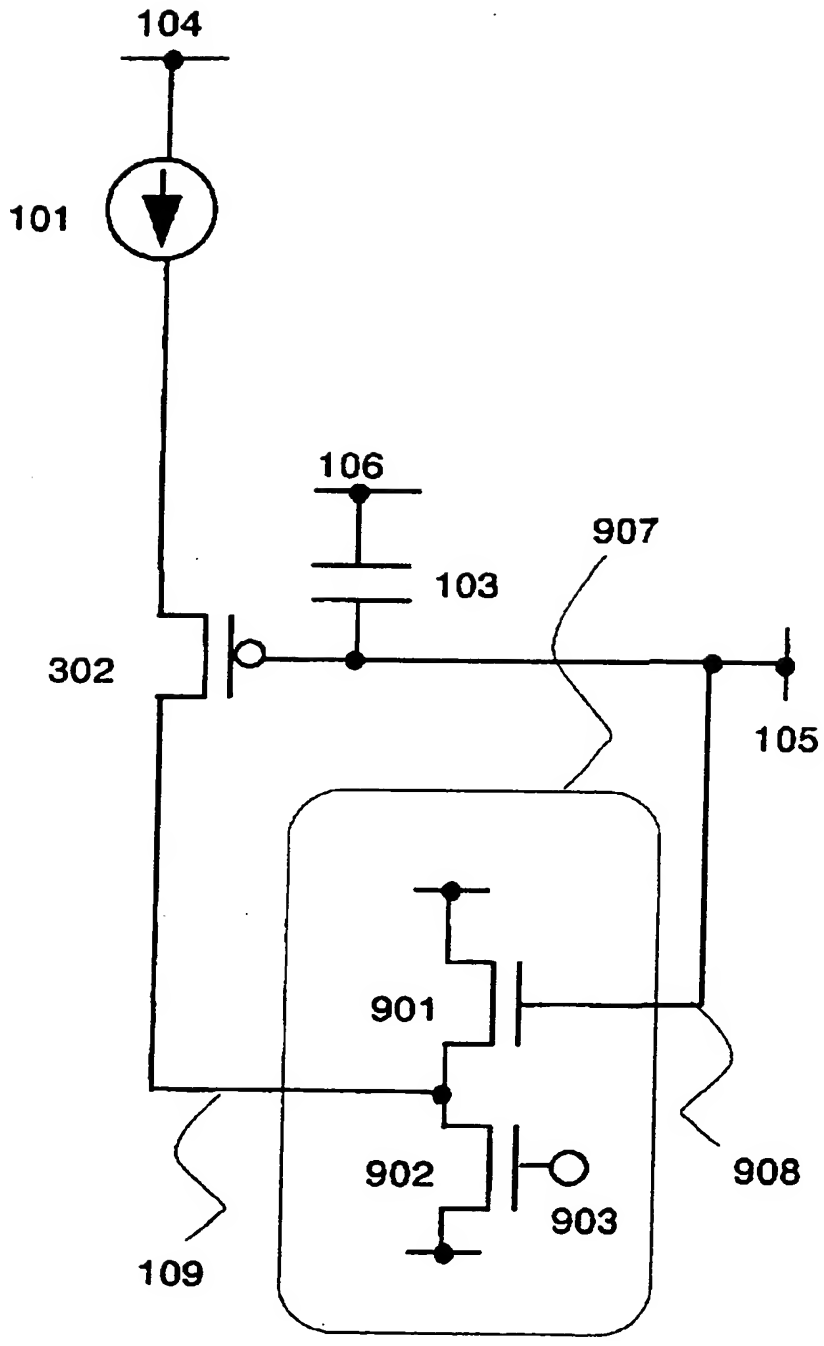
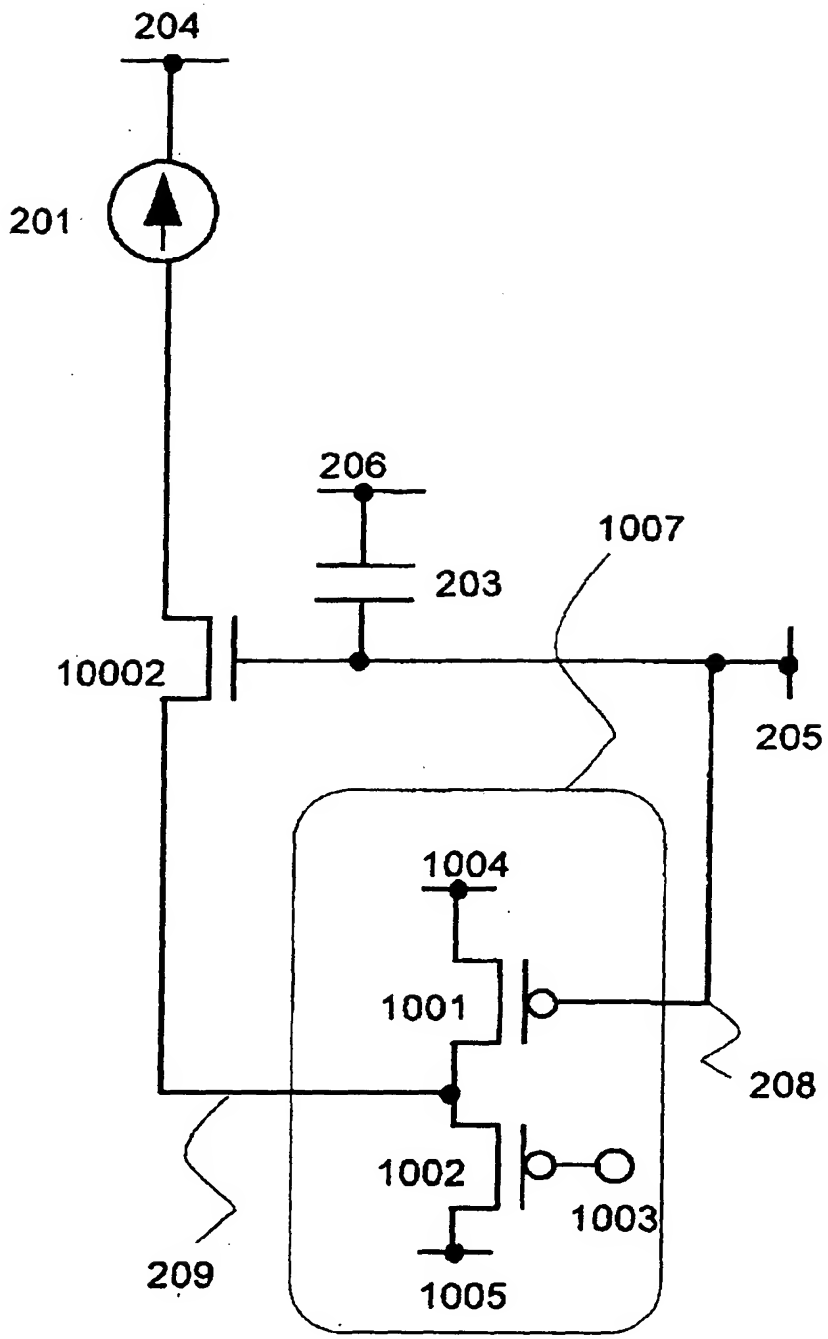


FIG. 9


204
201
206
203
1007
10002
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1004
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208
1002
1003
209
1005

FIG. 10

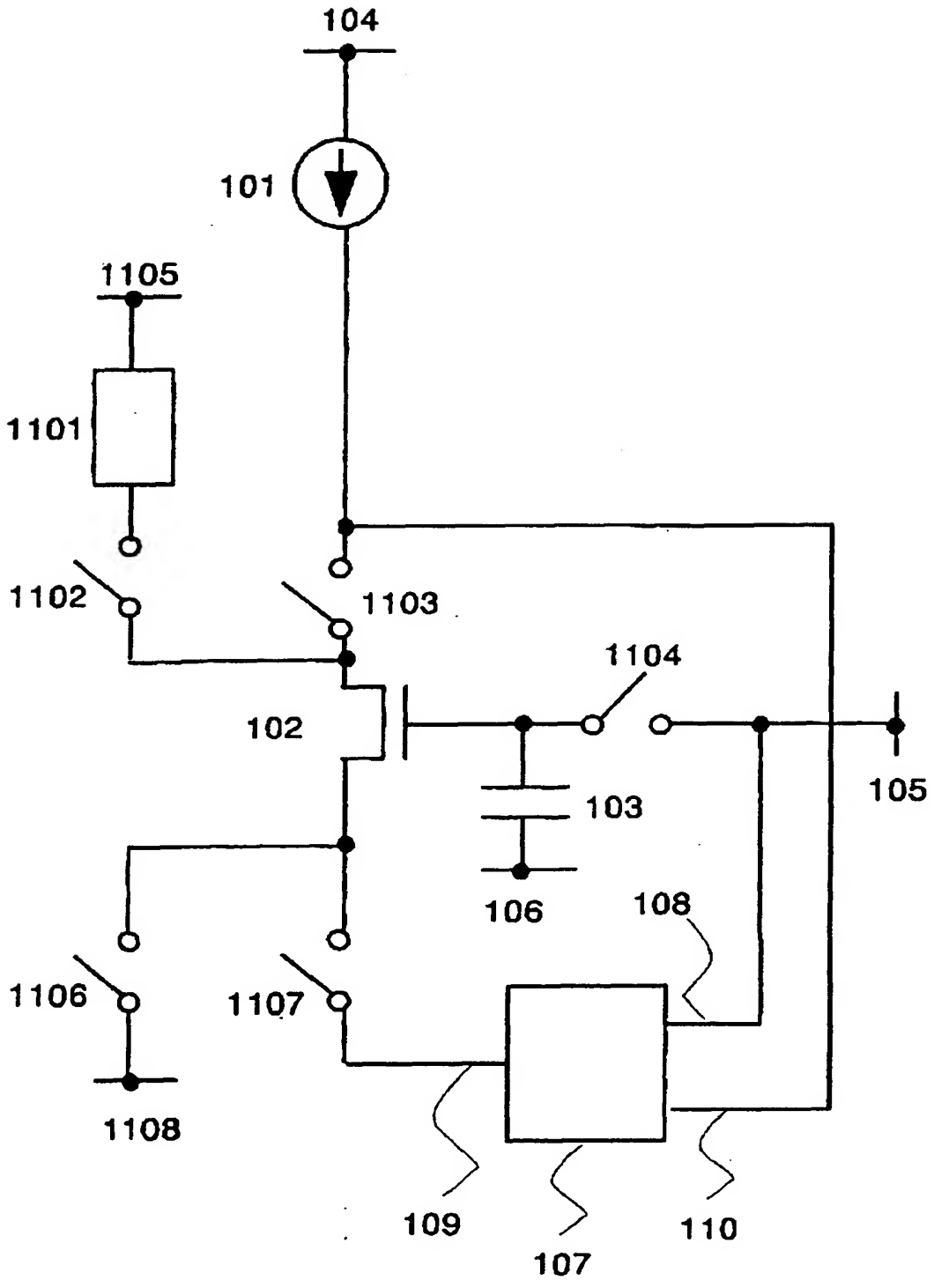
104
101
1105
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FIG. 11

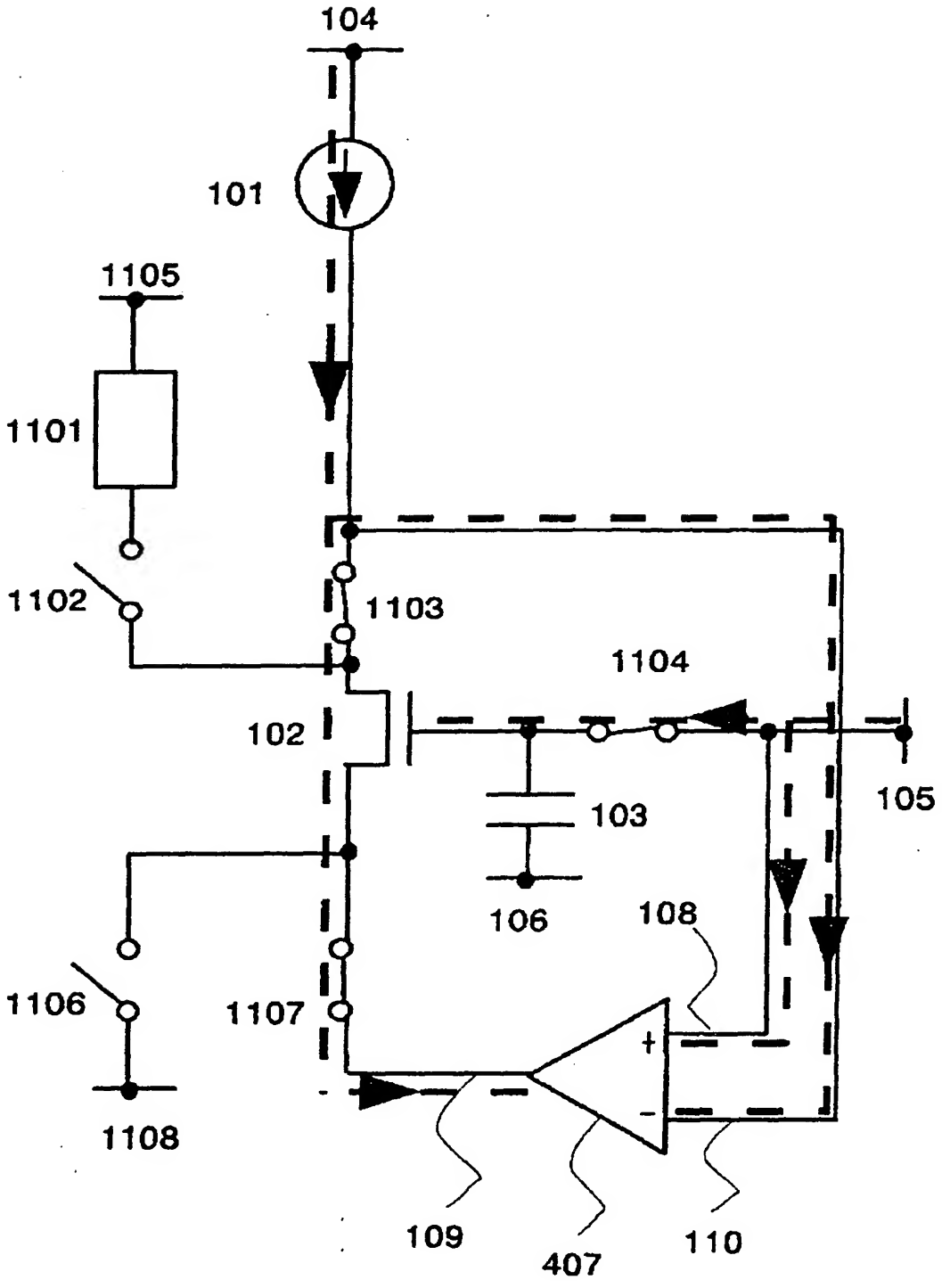
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FIG. 12

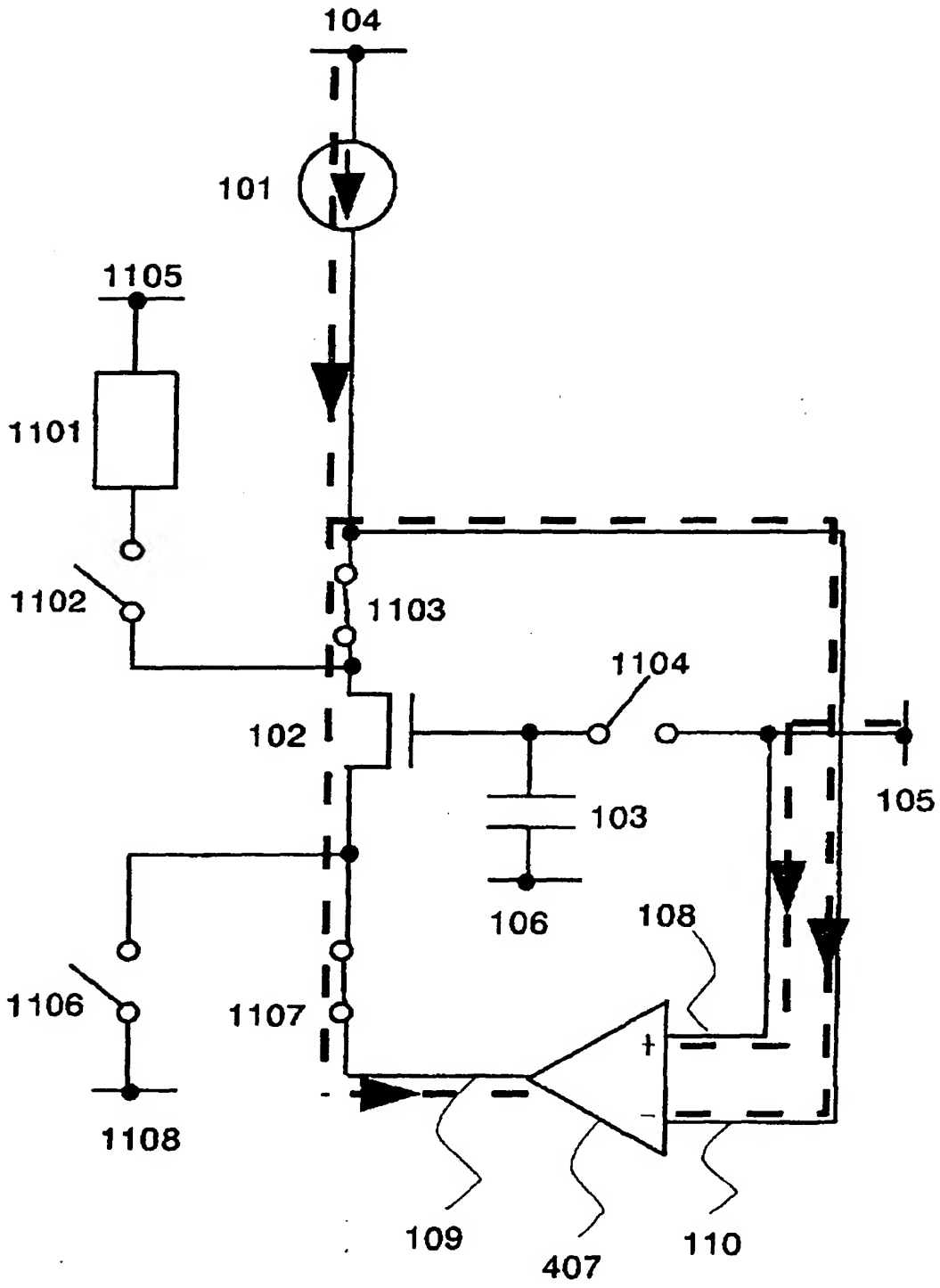
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FIG. 13

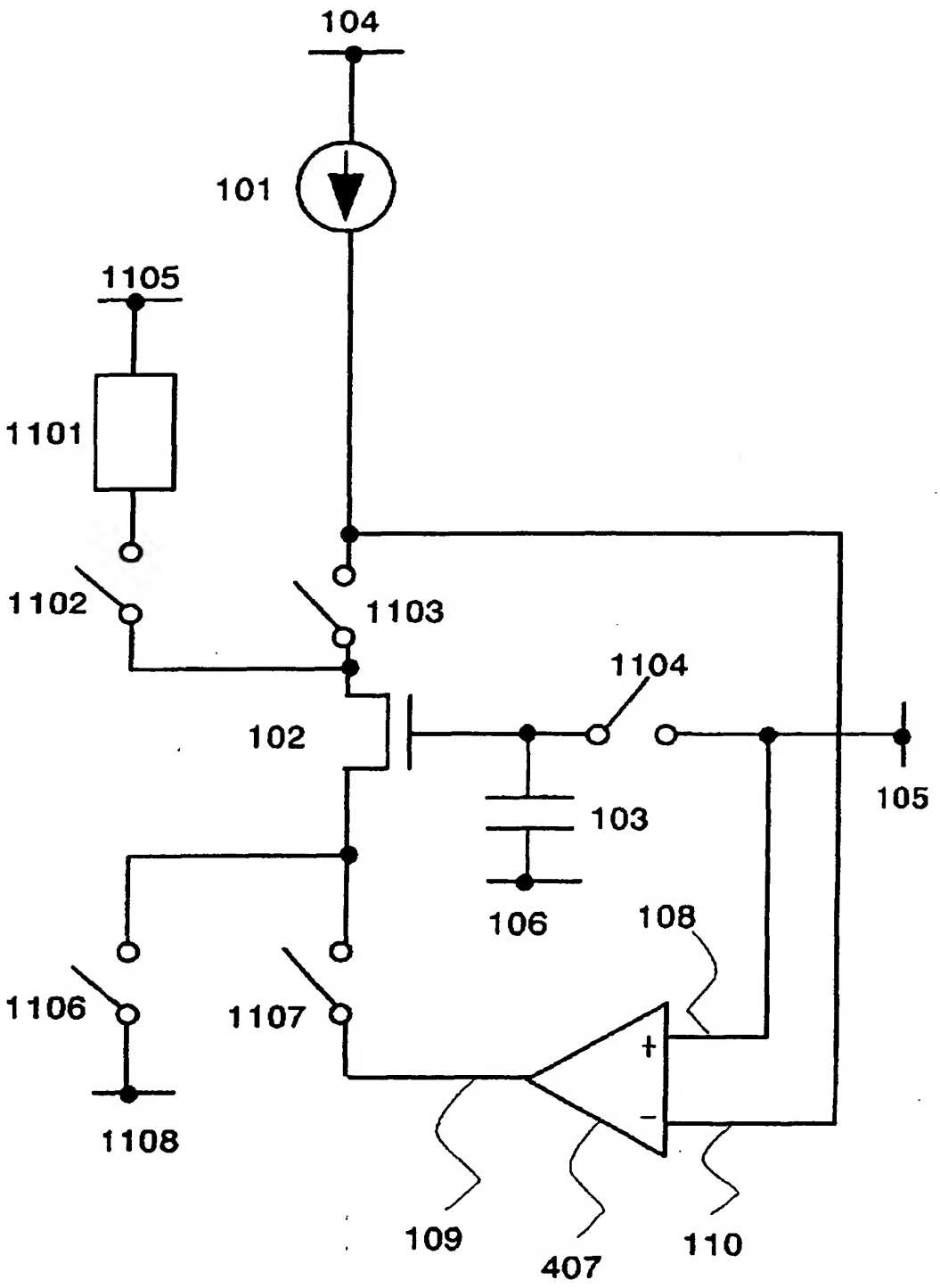
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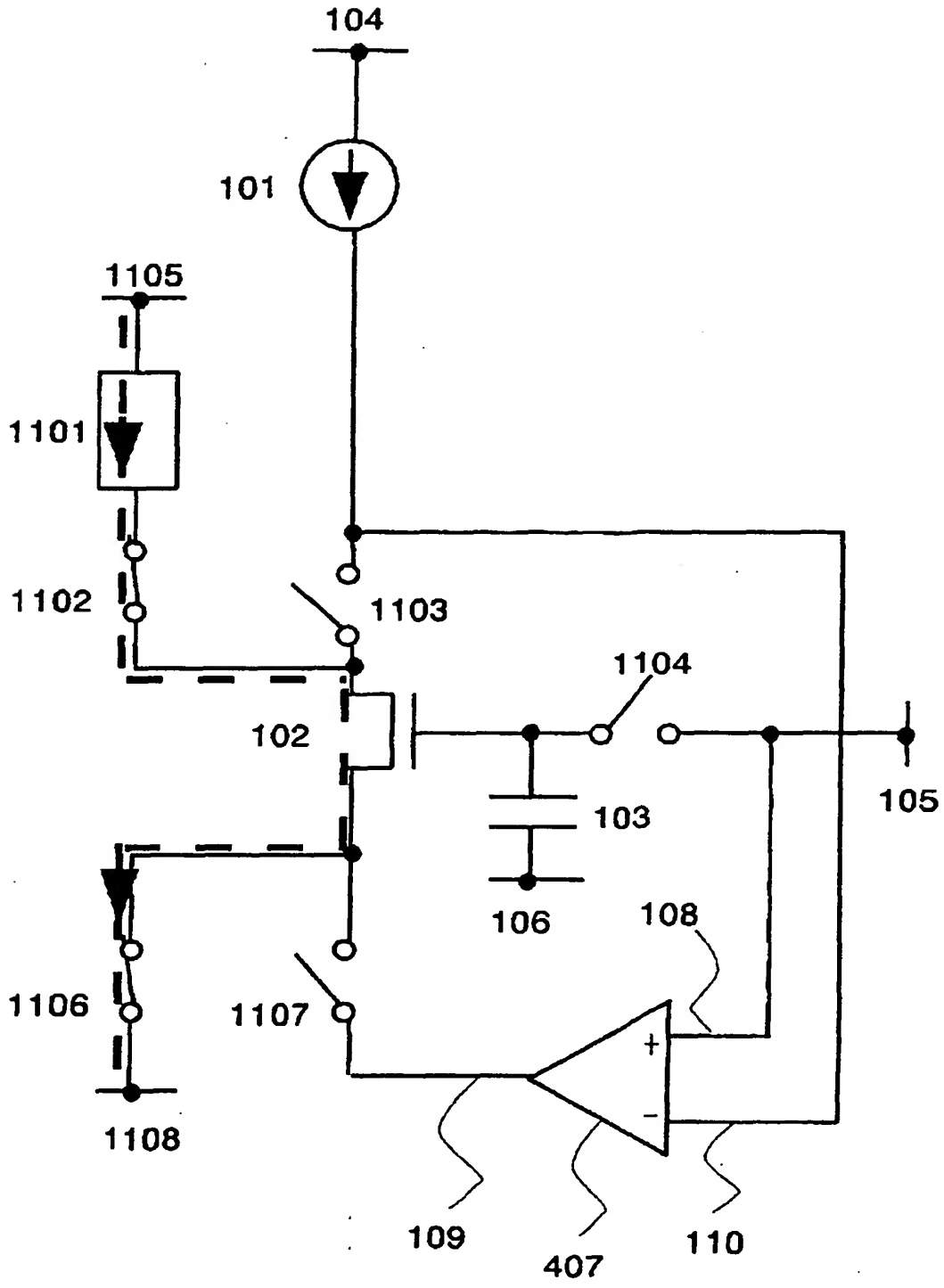
FIG. 14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407
110
+
-

FIG. 15

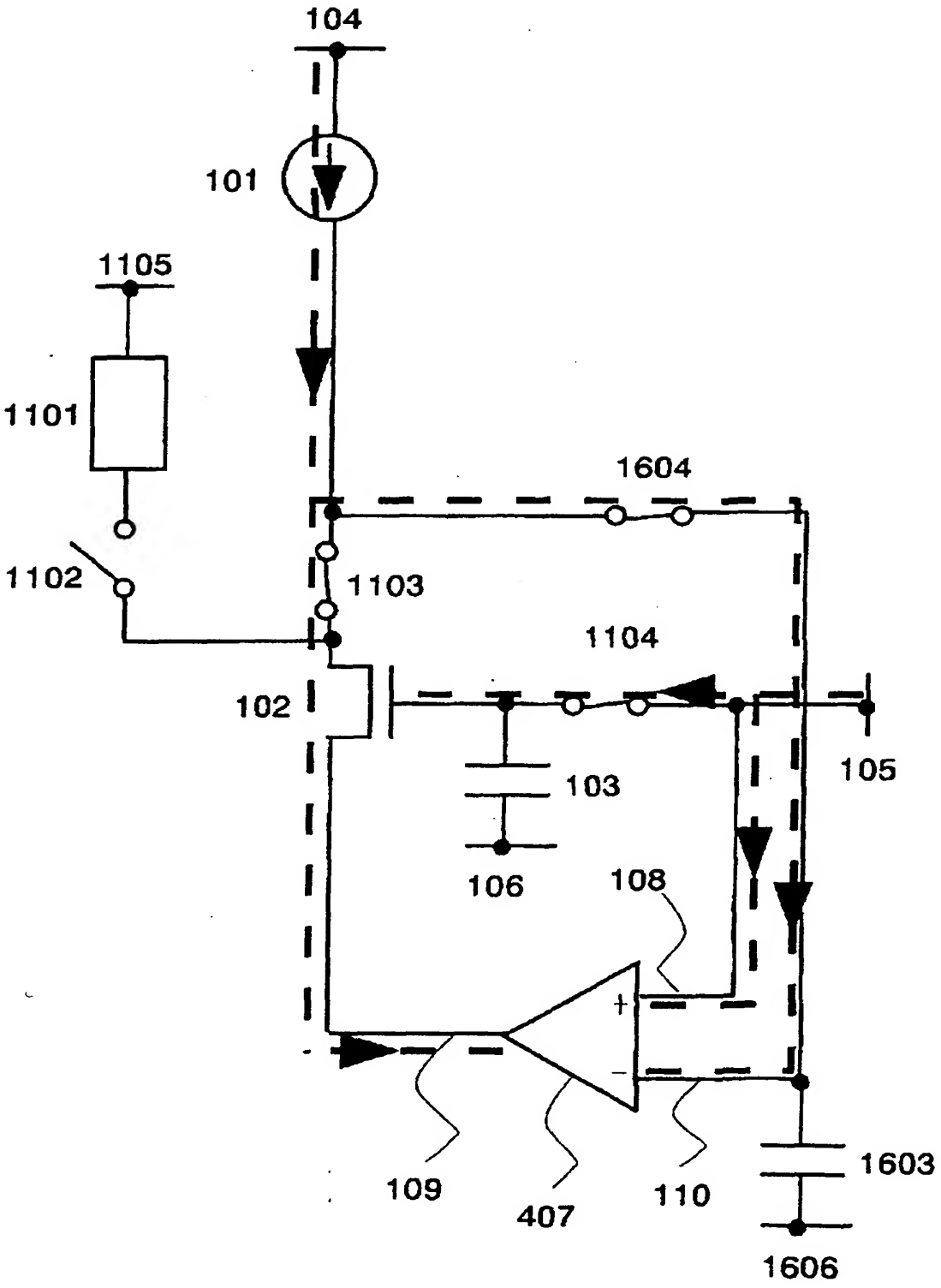

104
101
1105
1101
1604
1102
1103
1104
102
105
103
106
108
+
−
109
407
110
1603
1606

FIG. 16

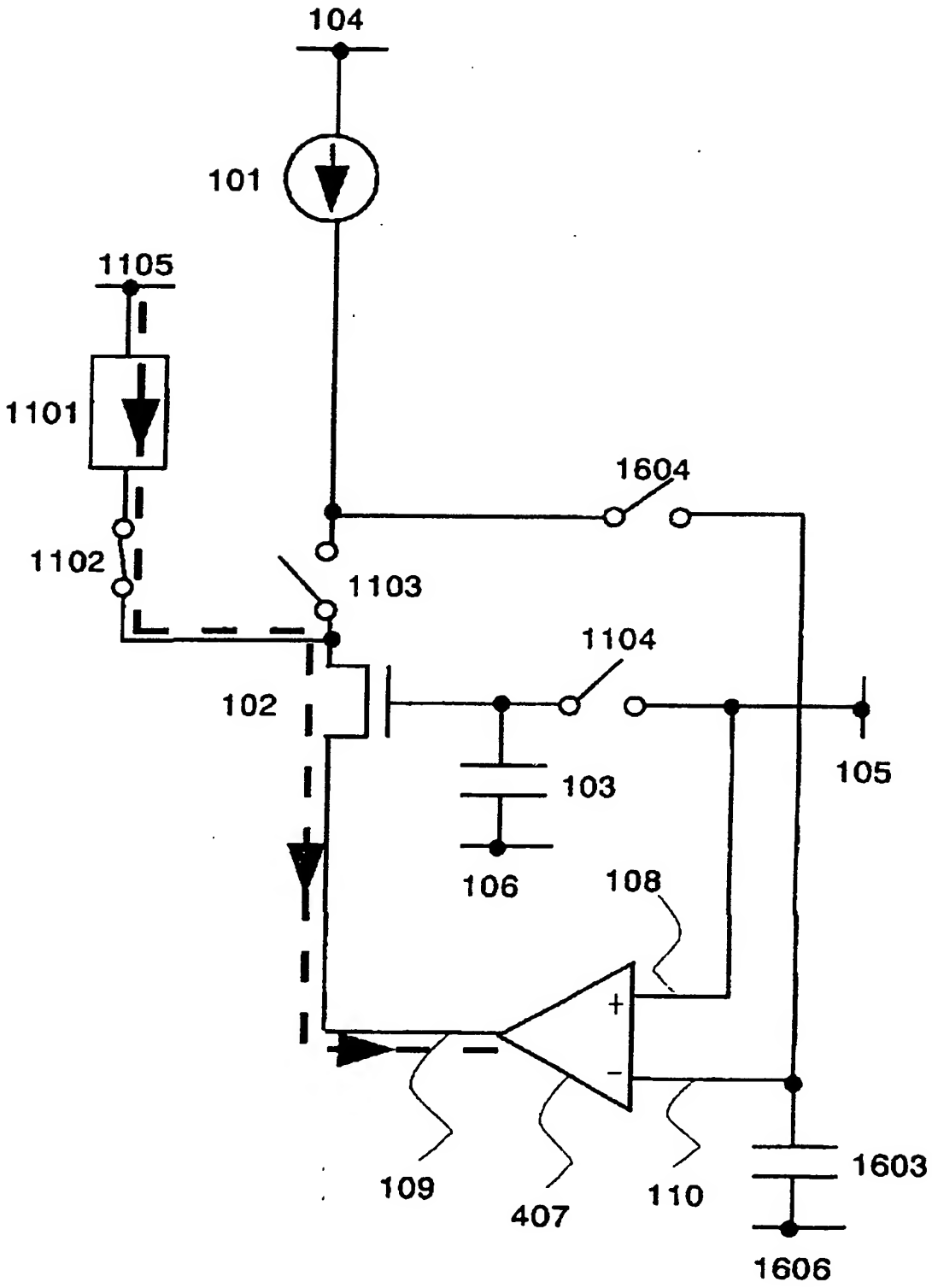

104
101
1105
1101
1604
1102
1103
1104
102
105
103
106
108
+
−
109
407
110
1603
1606

FIG. 17

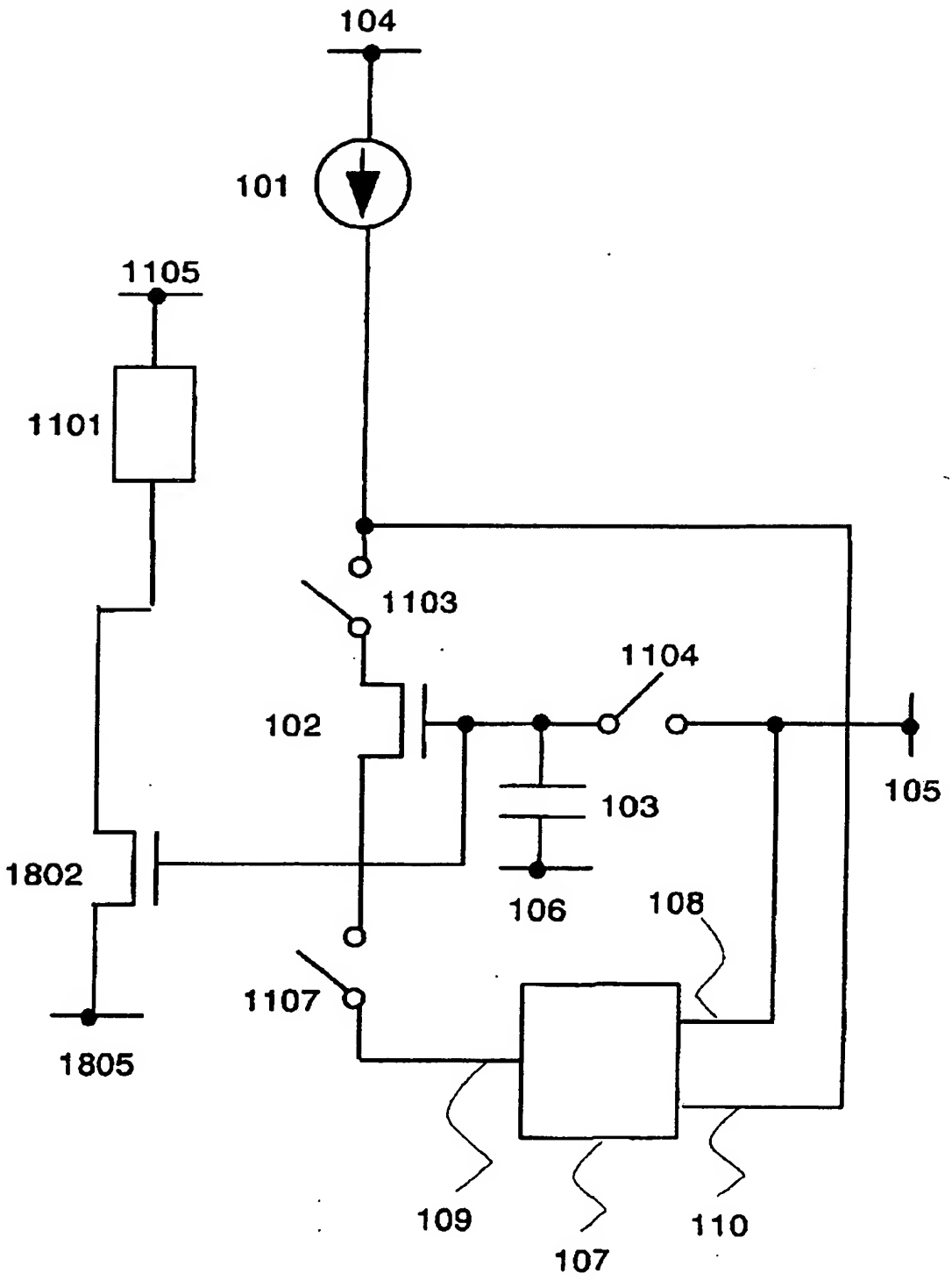

104
101
1105
1101
1103
1104
102
105
103
1802
106
108
1107
1805
109
107
110

FIG. 18

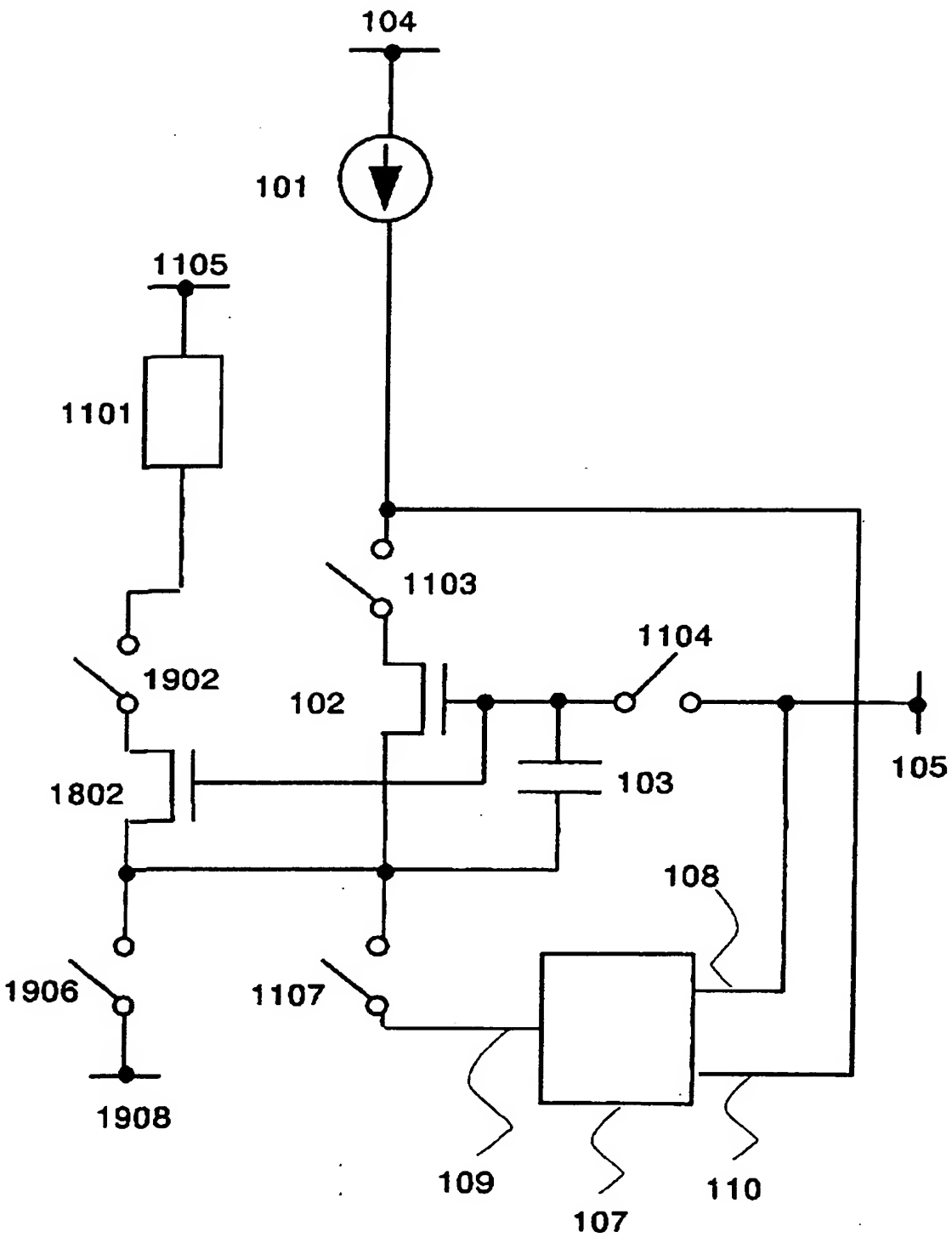

104
101
1105
1101
1103
1104
1902
102
105
1802
103
108
1906
1107
1908
109
107
110

FIG. 19

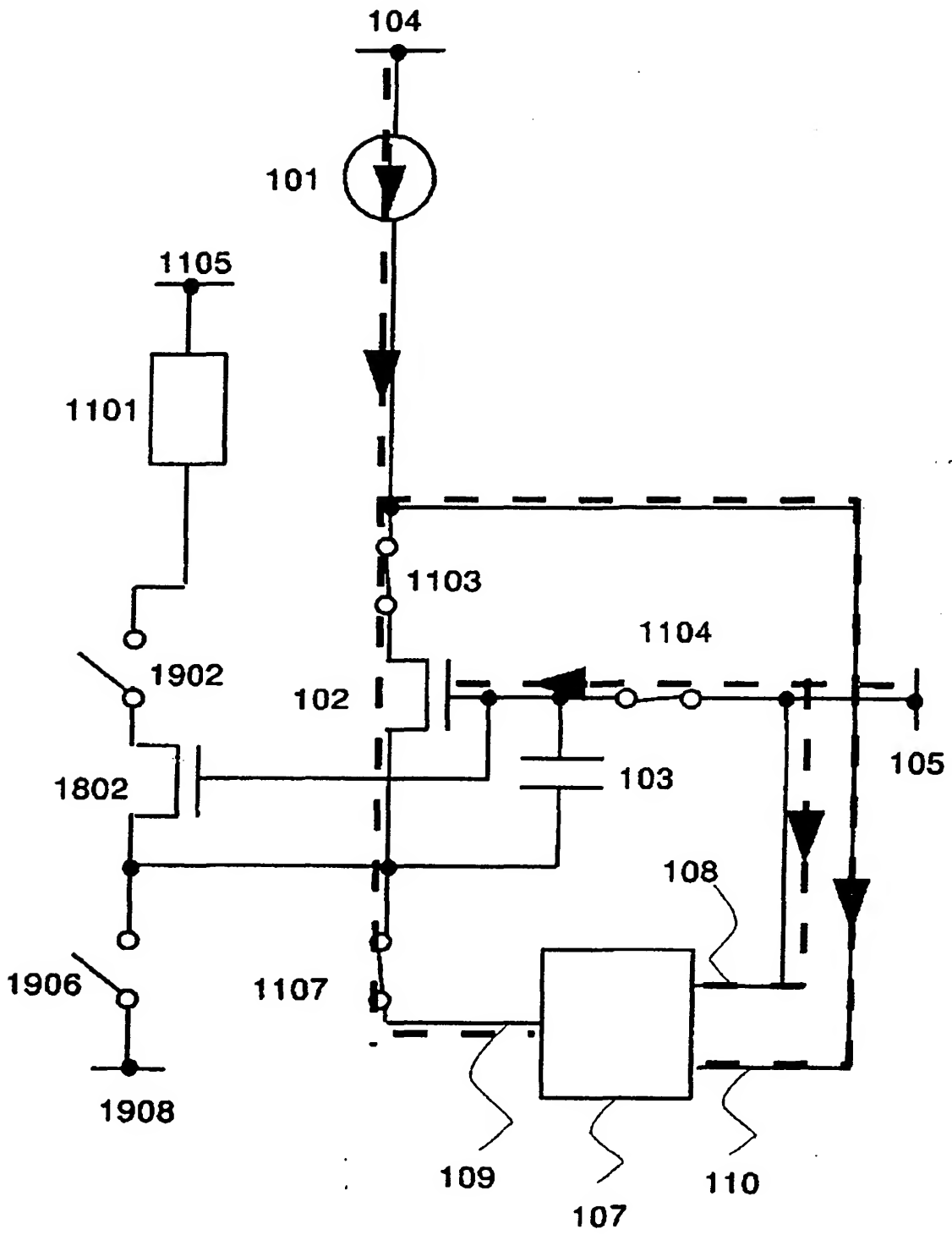

104
101
1105
1101
1103
1104
1902
102
105
1802
103
108
1906
1107
1908
109
107
110

FIG. 20

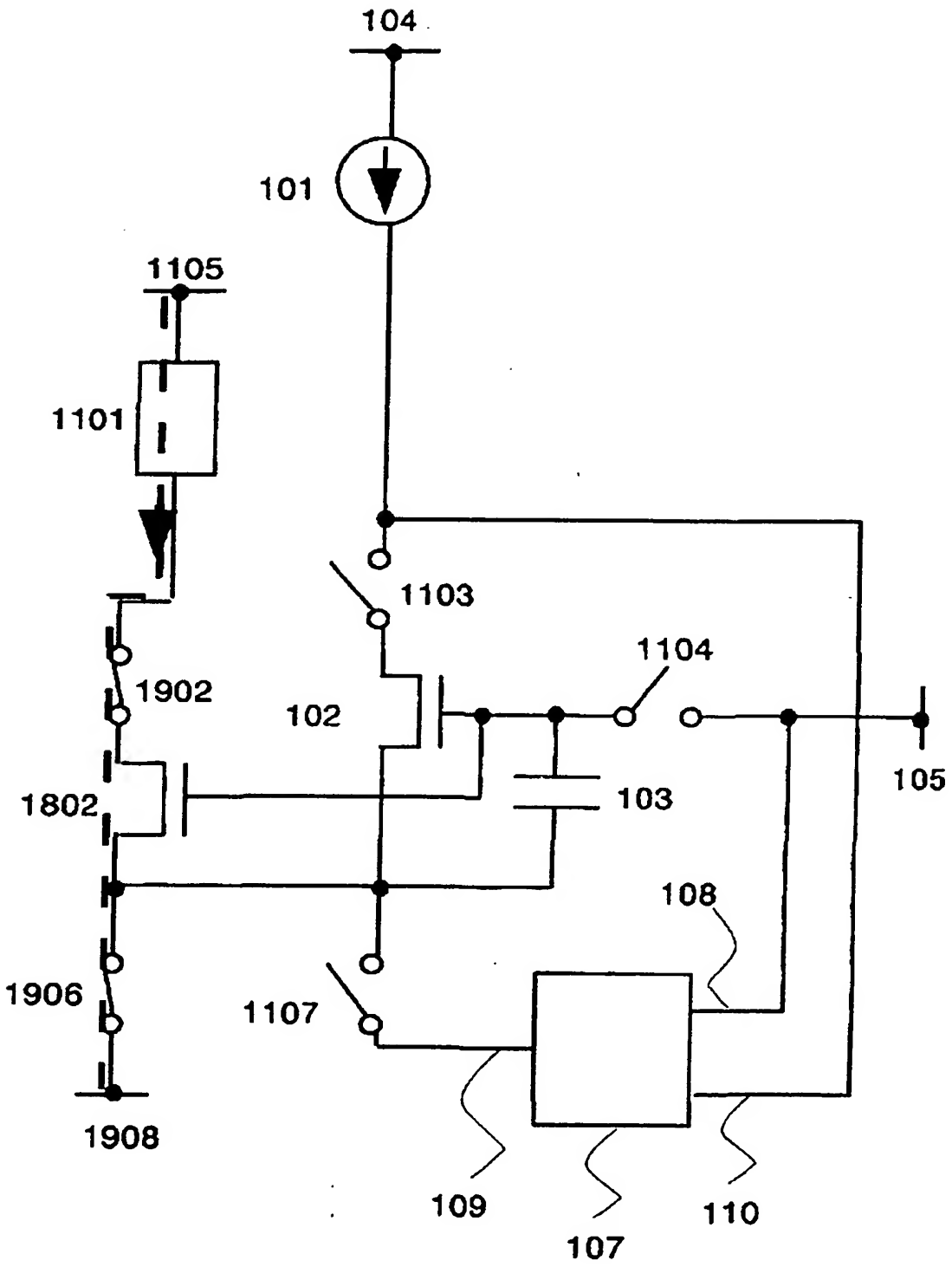

104
101
1105
1101
1103
1104
1902
102
105
1802
103
108
1906
1107
1908
109
107
110

FIG. 21

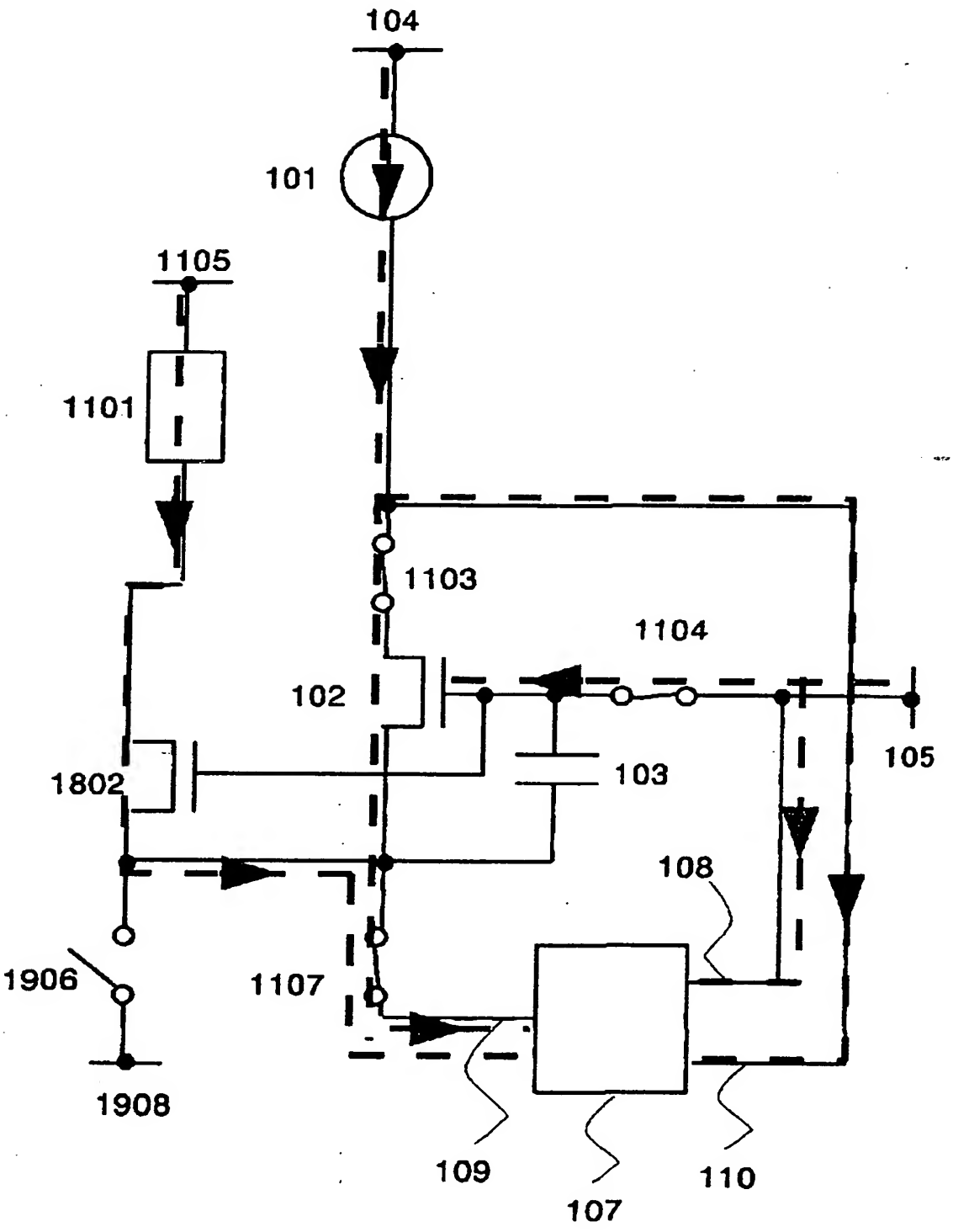

104
101
1105
1101
1103
1104
102
105
103
1802
108
1906
1107
1908
109
107
110

FIG. 22

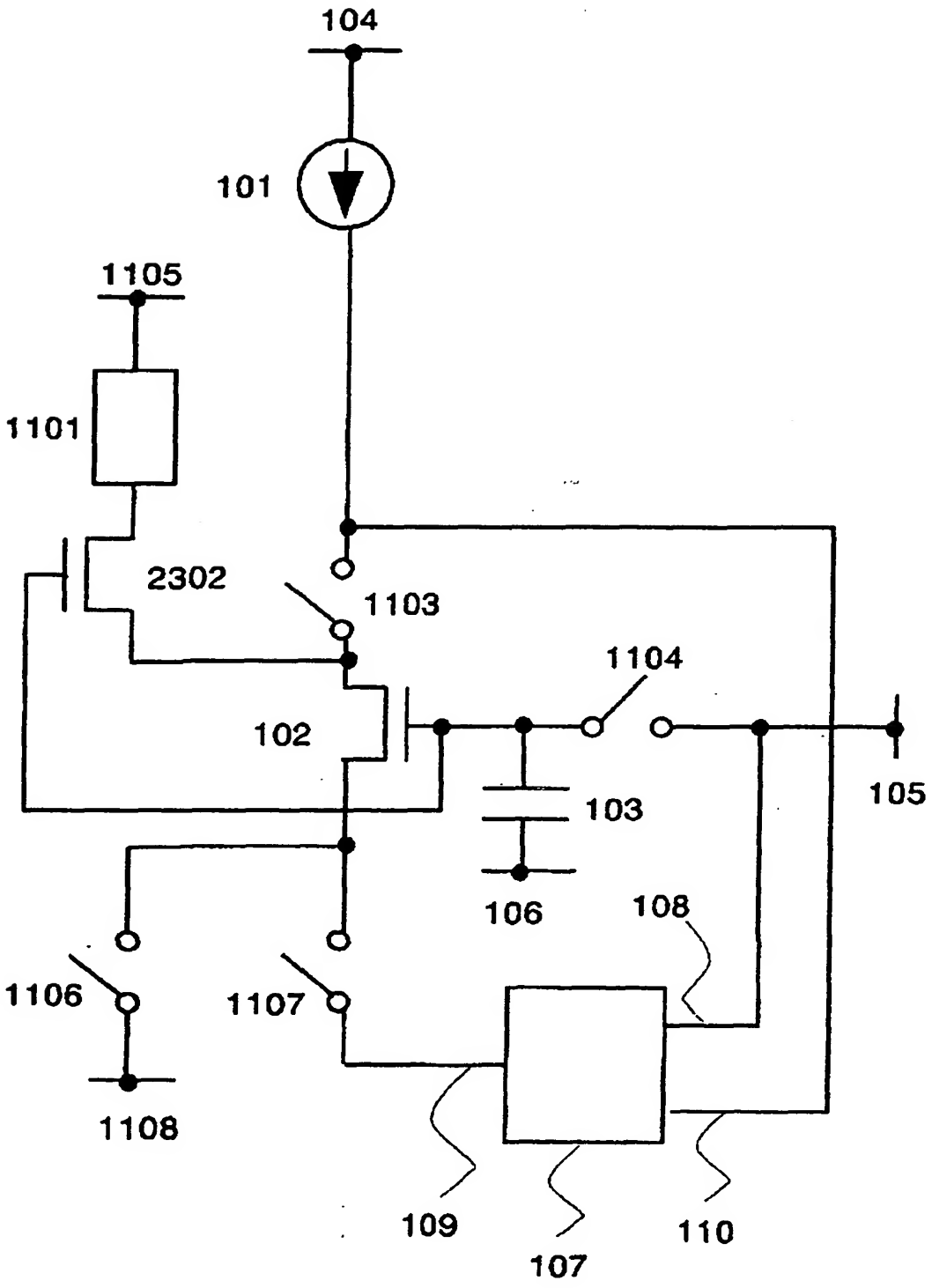

104
101
1105
1101
2302
1103
1104
102
103
105
106
108
1106
1107
1108
109
107
110

FIG. 23

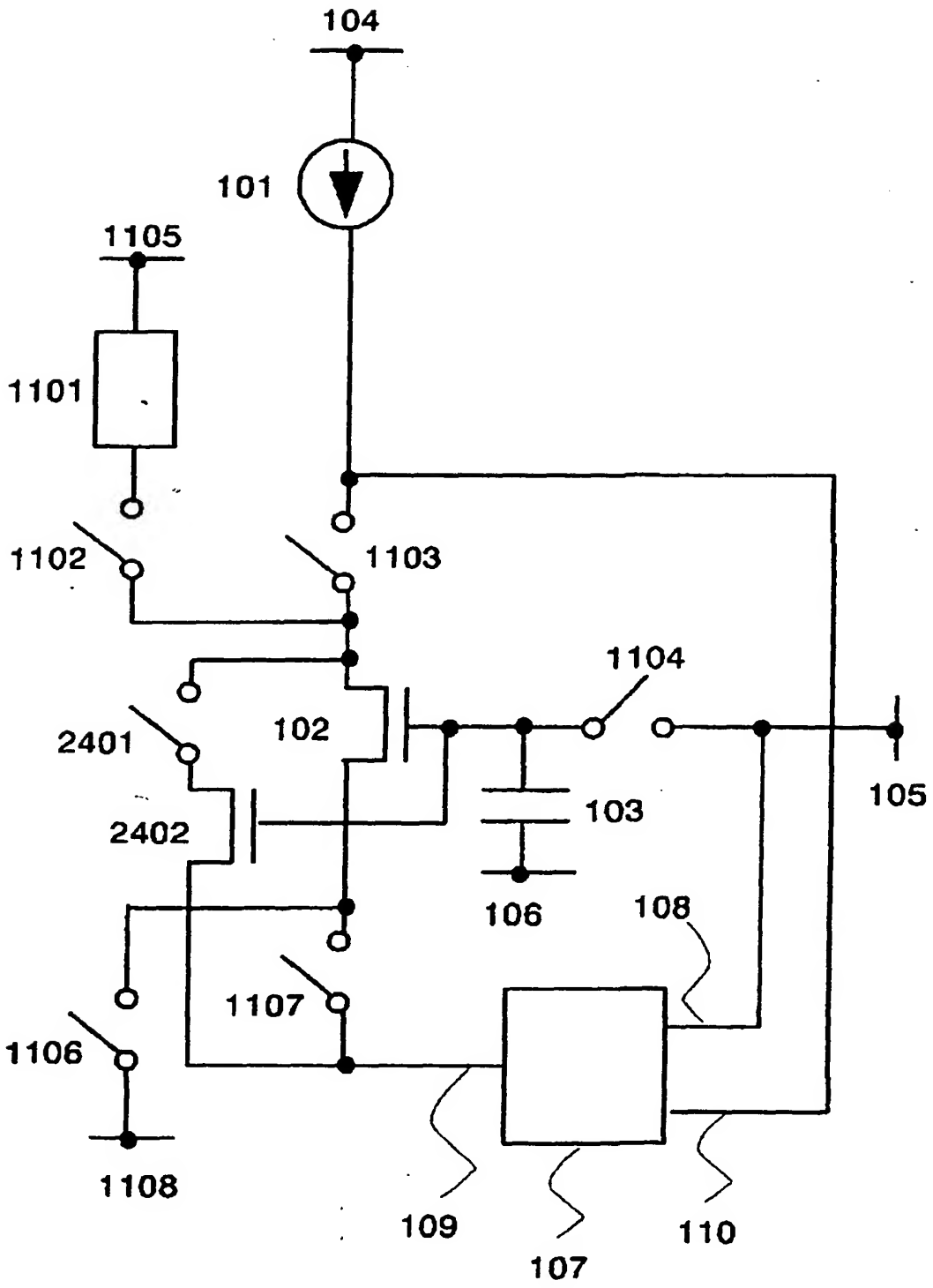

104
101
1105
1101
1102
1103
1104
2401
102
105
2402
103
106
108
1107
1106
1108
109
107
110

FIG. 24

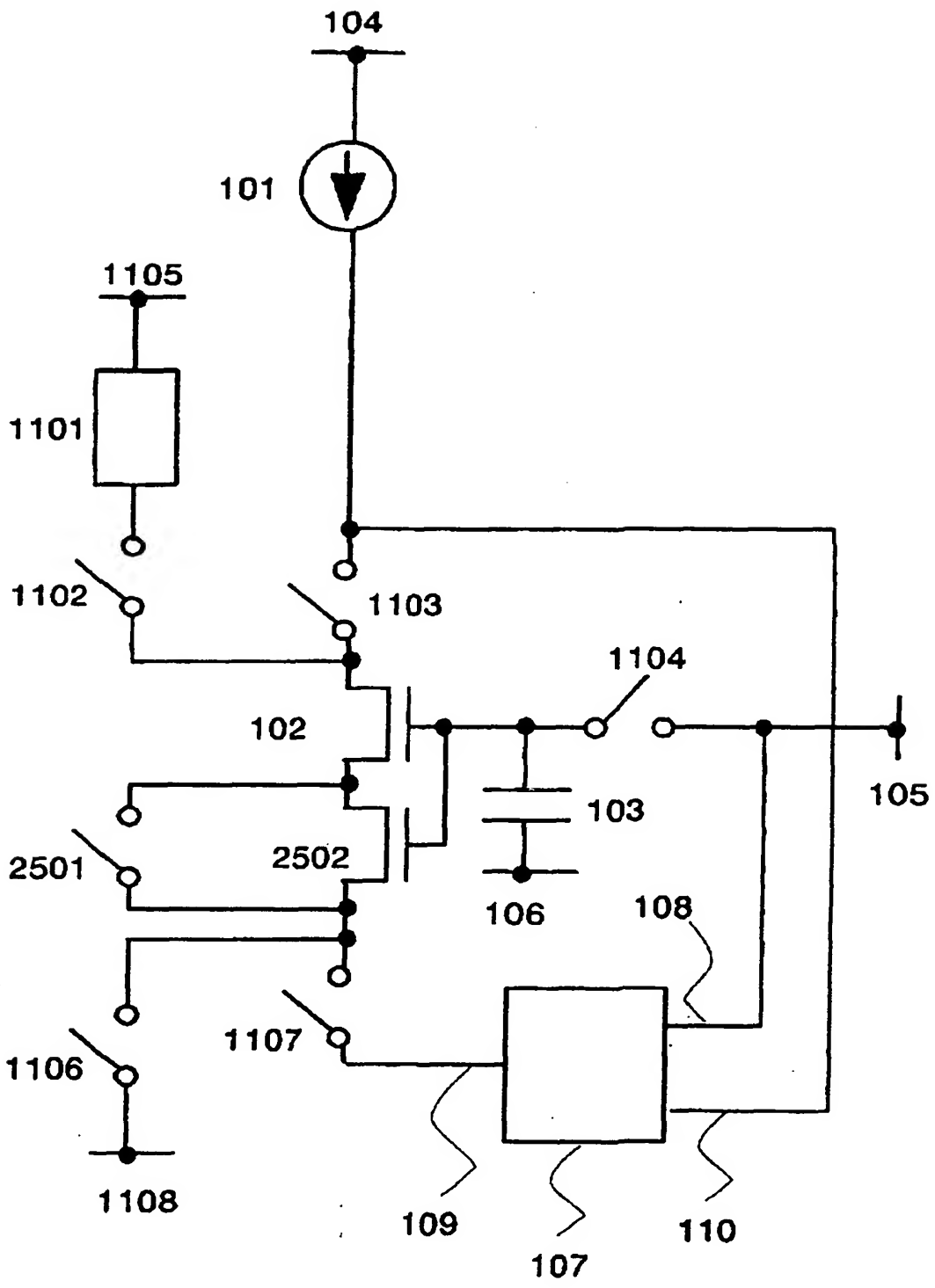

104
101
1105
1101
1102
1103
1104
102
105
103
2501
2502
106
108
1107
1106
1108
109
107
110

FIG. 25

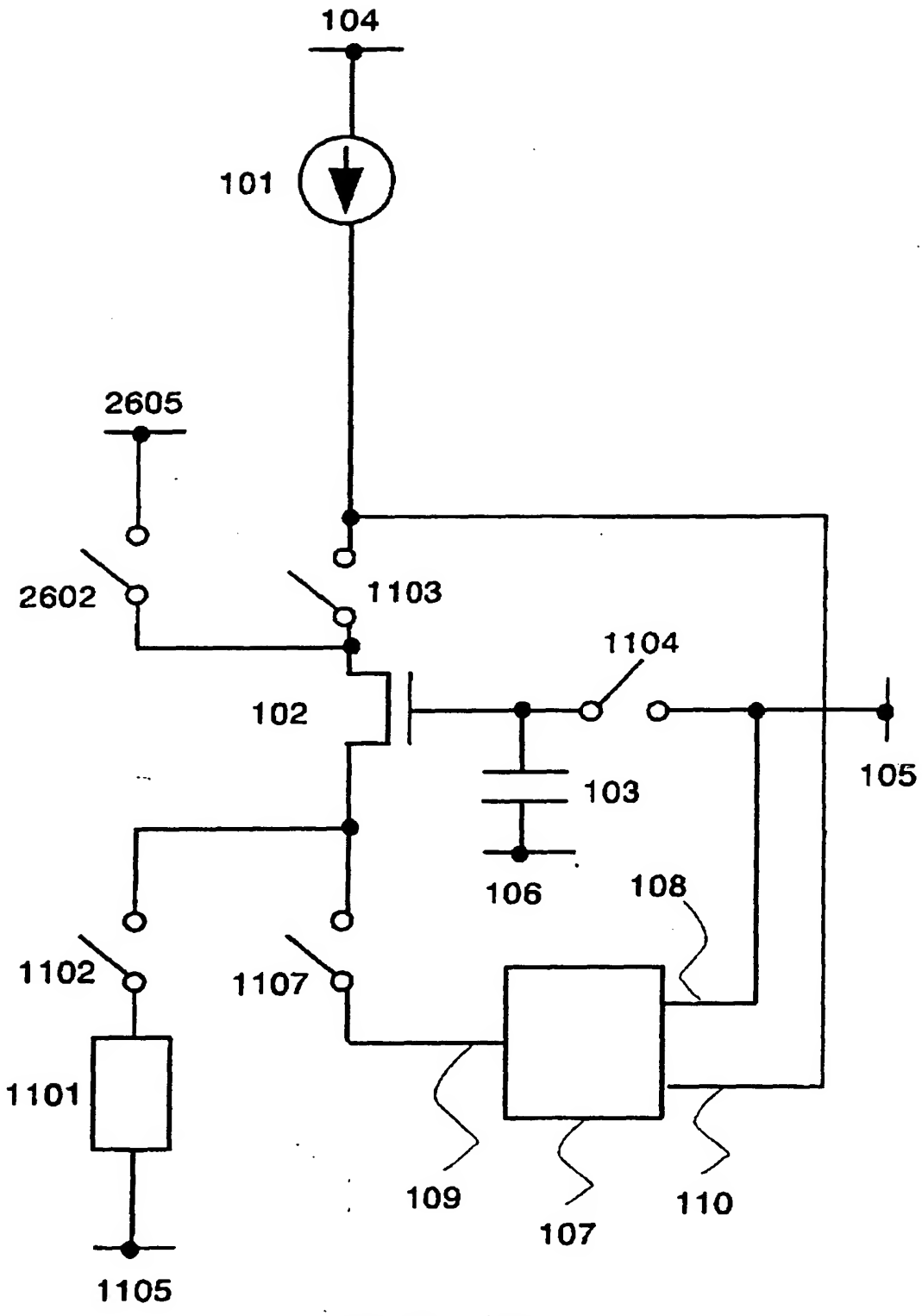

104
101
2605
2602
1103
1104
102
105
103
106
108
1102
1107
1101
109
107
110
1105

FIG. 26

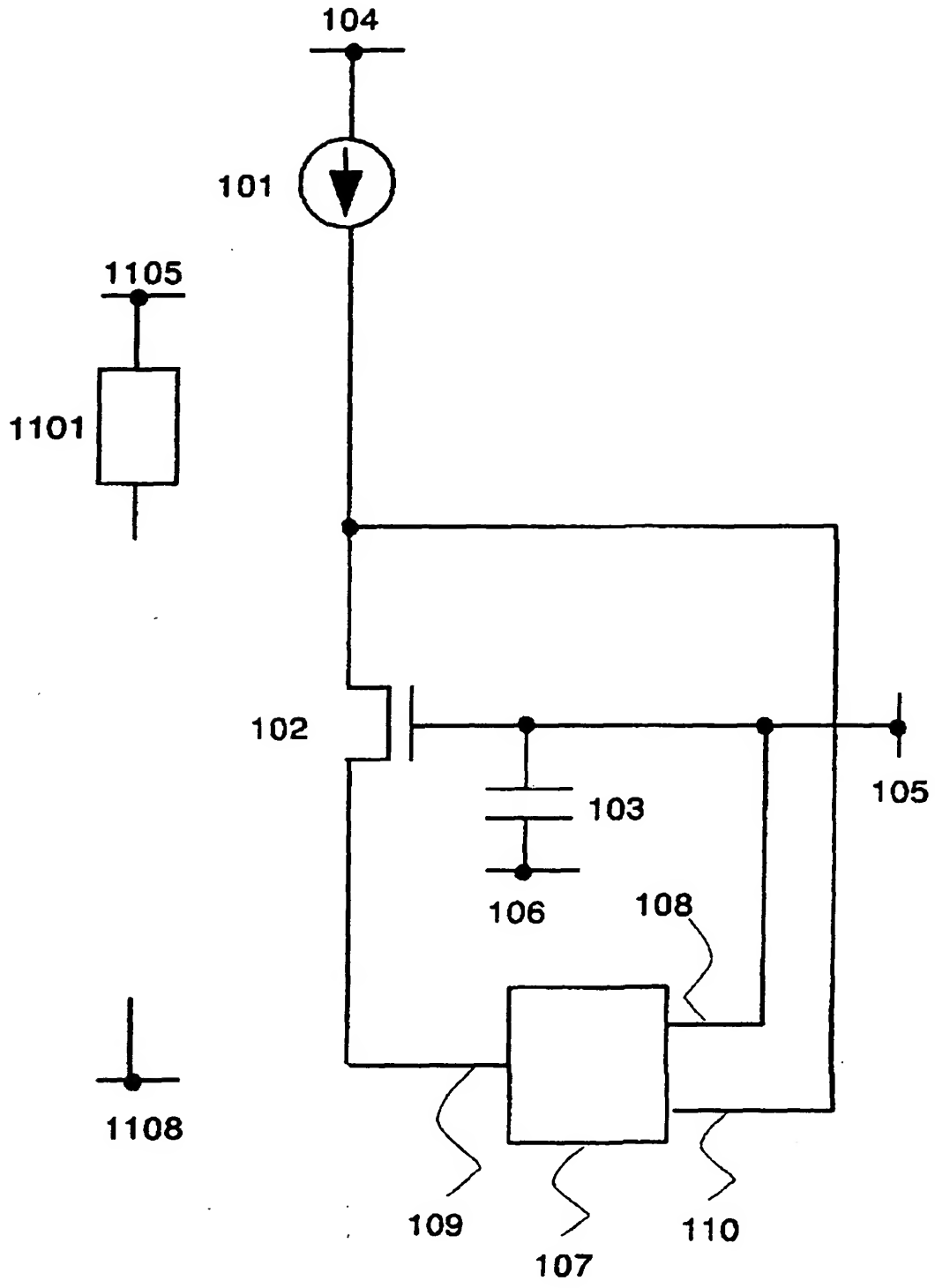


FIG. 27

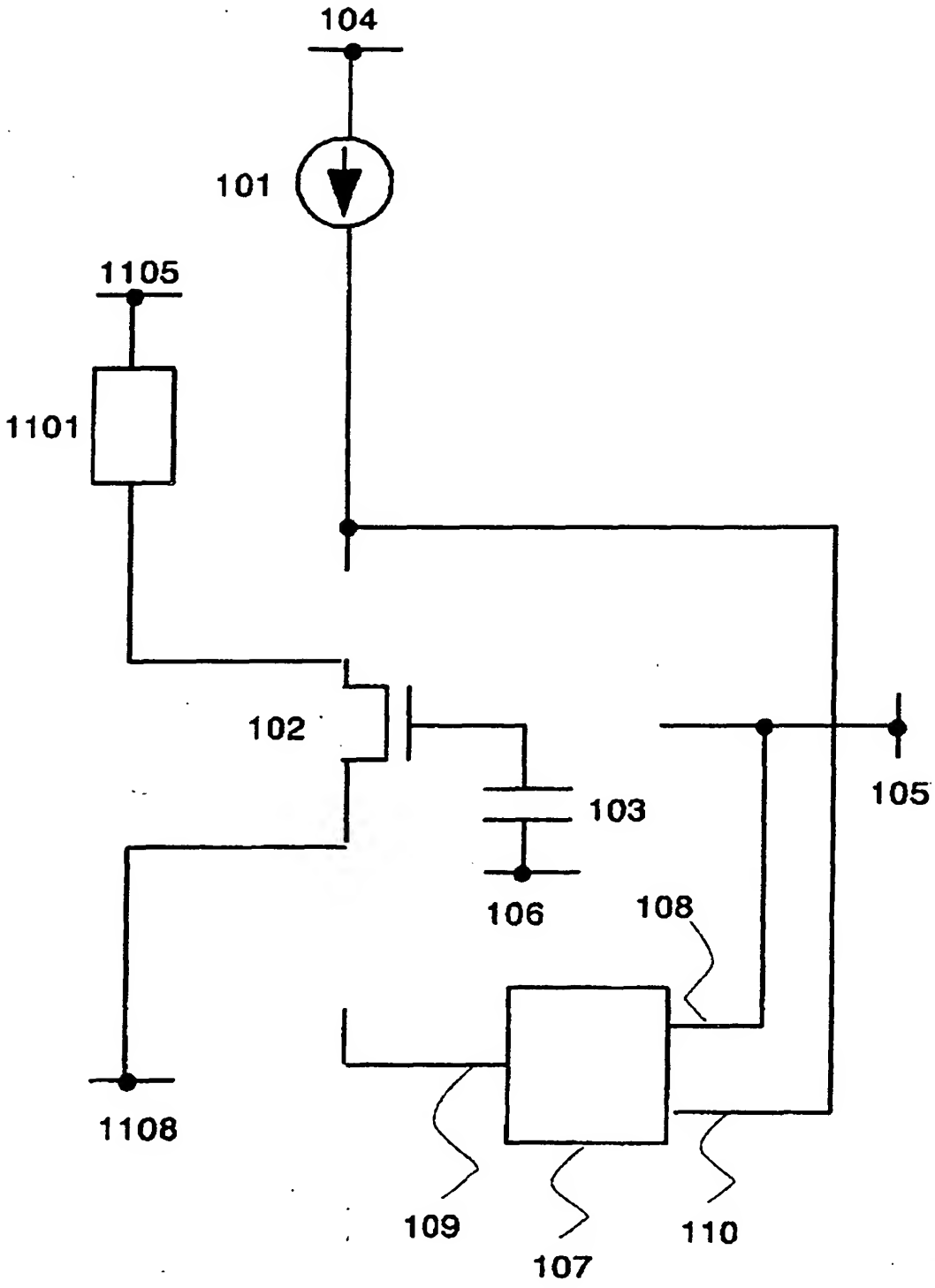


FIG. 28

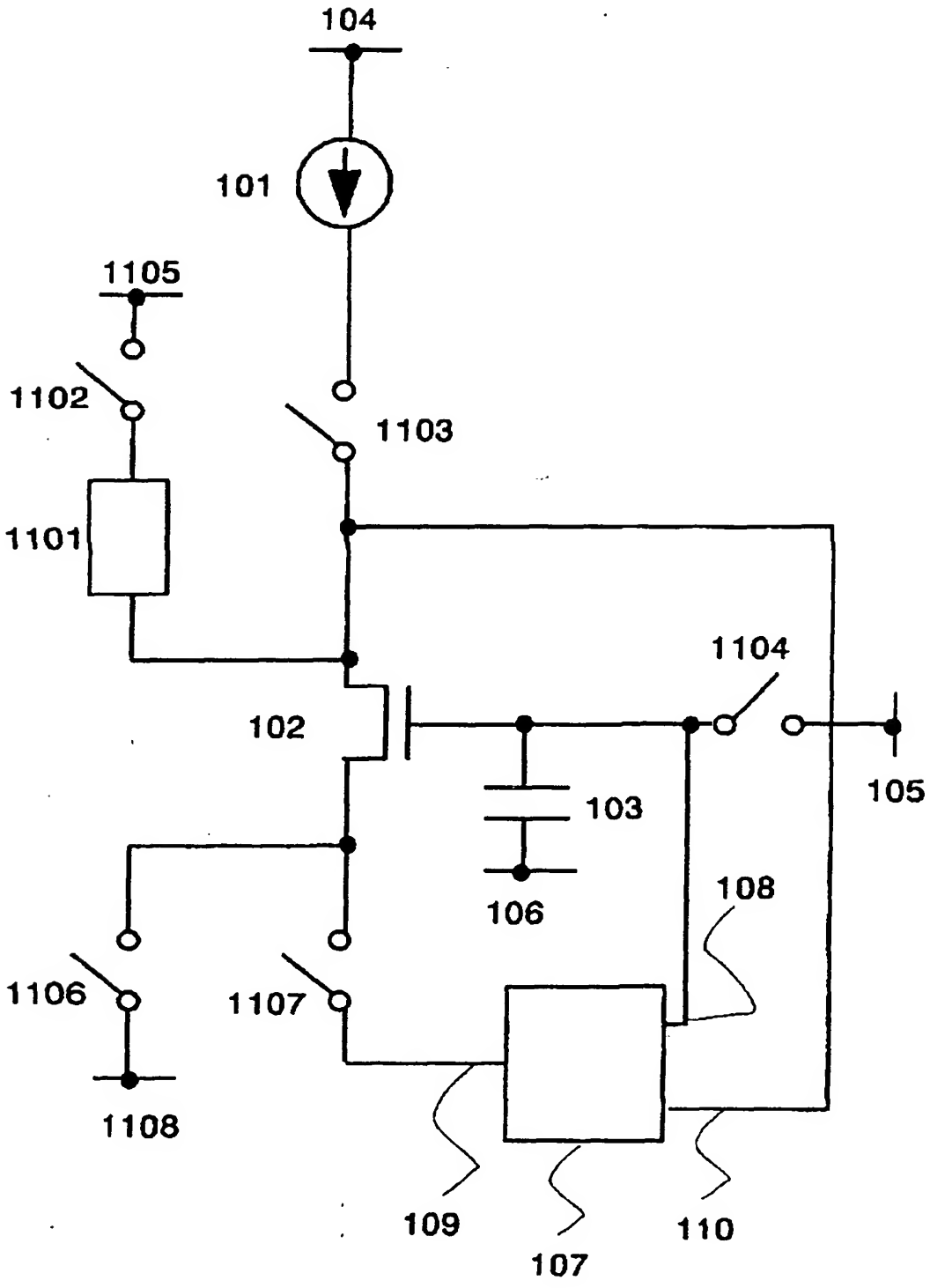
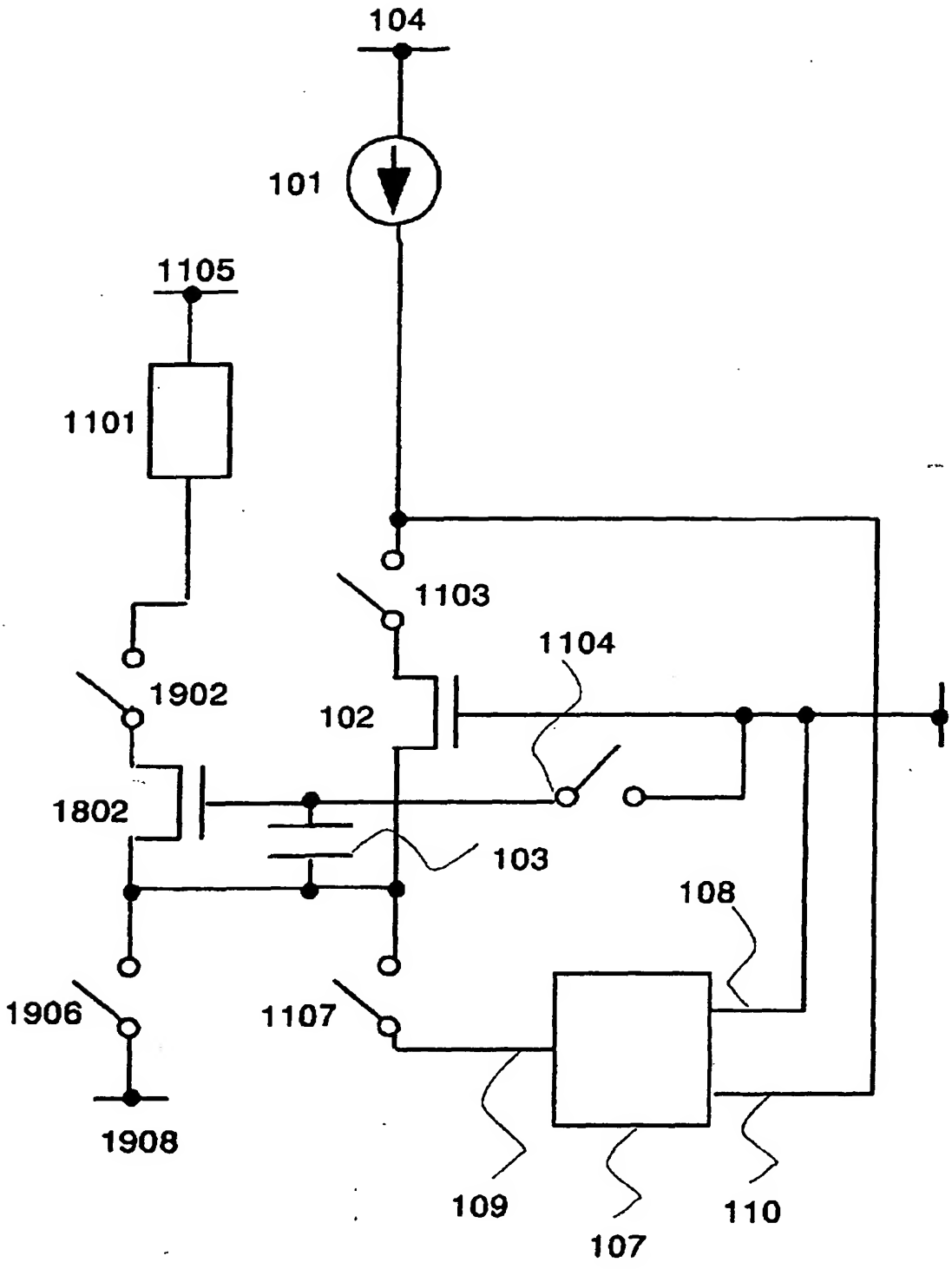

104
101
1105
1102
1103
1101
1104
102
105
103
106
108
1106
1107
1108
109
107
110

FIG. 29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101
1105
1101
1103
1104
1902
102
1802
103
108
1906
1107
1908
109
107
110

FIG. 30

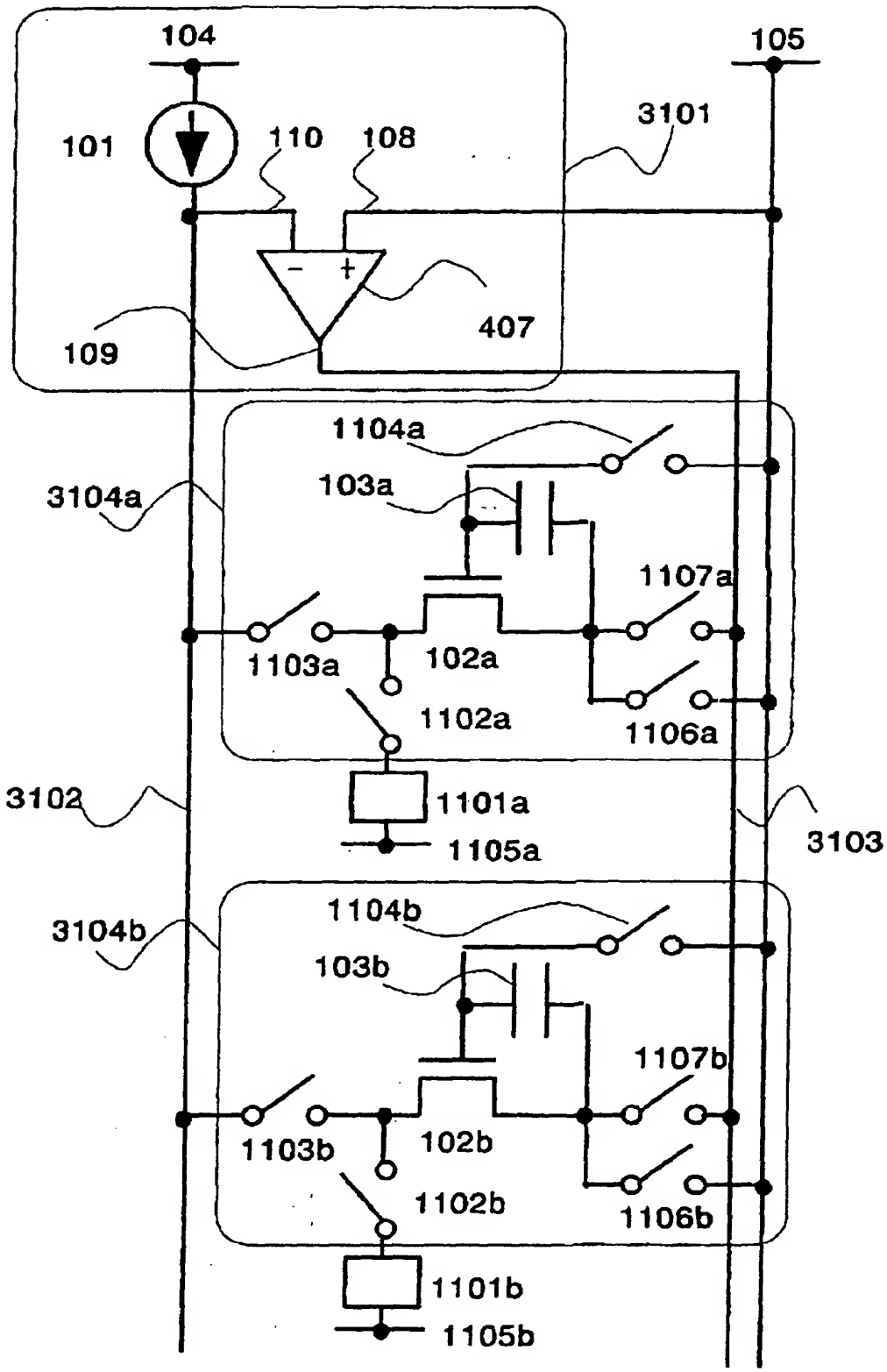
104
105
101
110
108
3101
407
109
1104a
3104a
103a
1107a
1103a
102a
1102a
1106a
3102
1101a
1105a
3103
1104b
3104b
103b
1107b
1103b
102b
1102b
1106b
1101b
1105b

FIG. 31

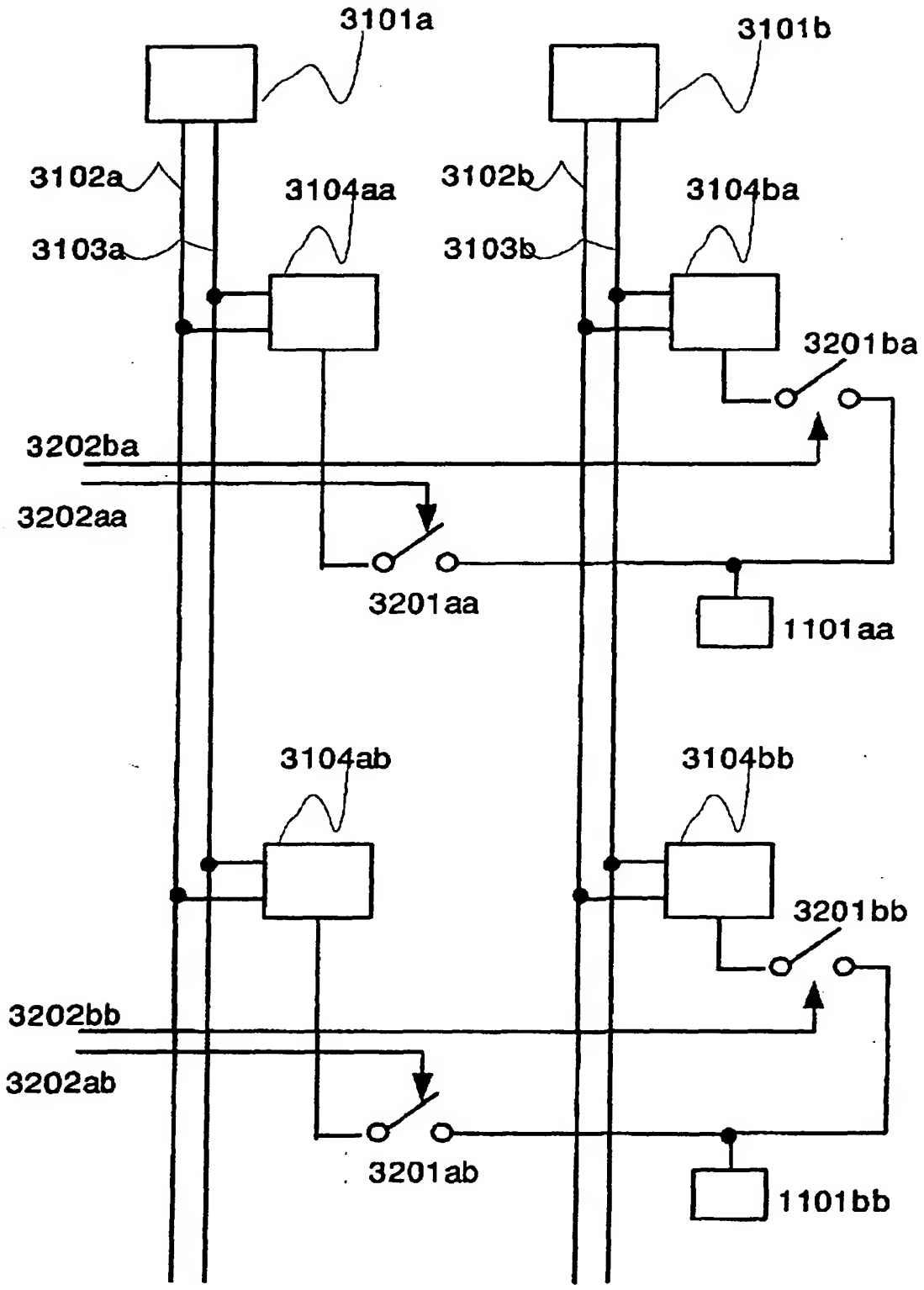
3101a
3101b
3102a
3104aa
3102b
3104ba
3103a
3103b
3201ba
3202ba
3202aa
3201aa
1101aa
3104ab
3104bb
3201bb
3202bb
3202ab
3201ab
1101bb

FIG. 32

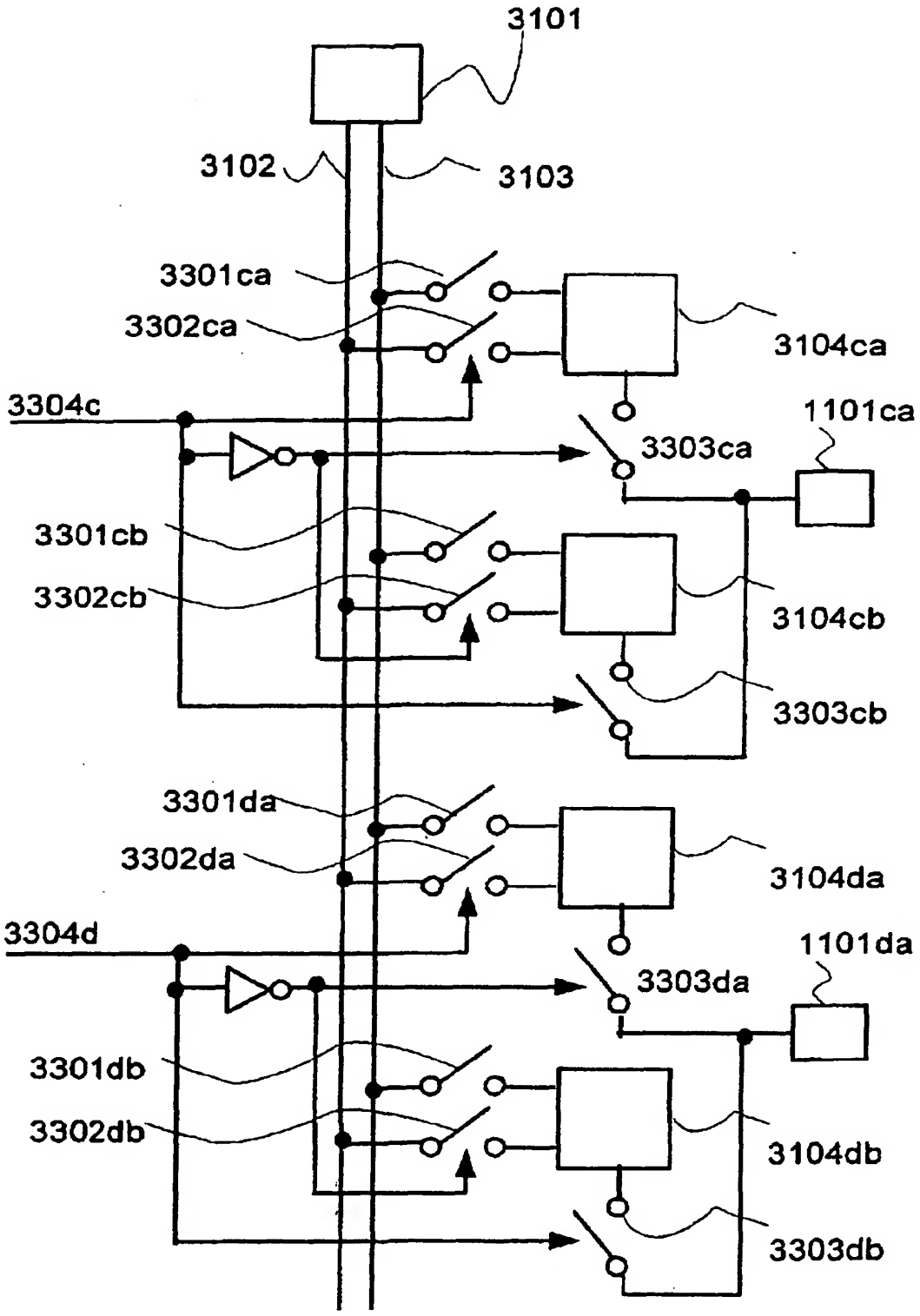
3101
3102
3103
3301ca
3302ca
3104ca
3304c
1101ca
3303ca
3301cb
3302cb
3104cb
3303cb
3301da
3302da
3104da
3304d
1101da
3303da
3301db
3302db
3104db
3303db

FIG. 33

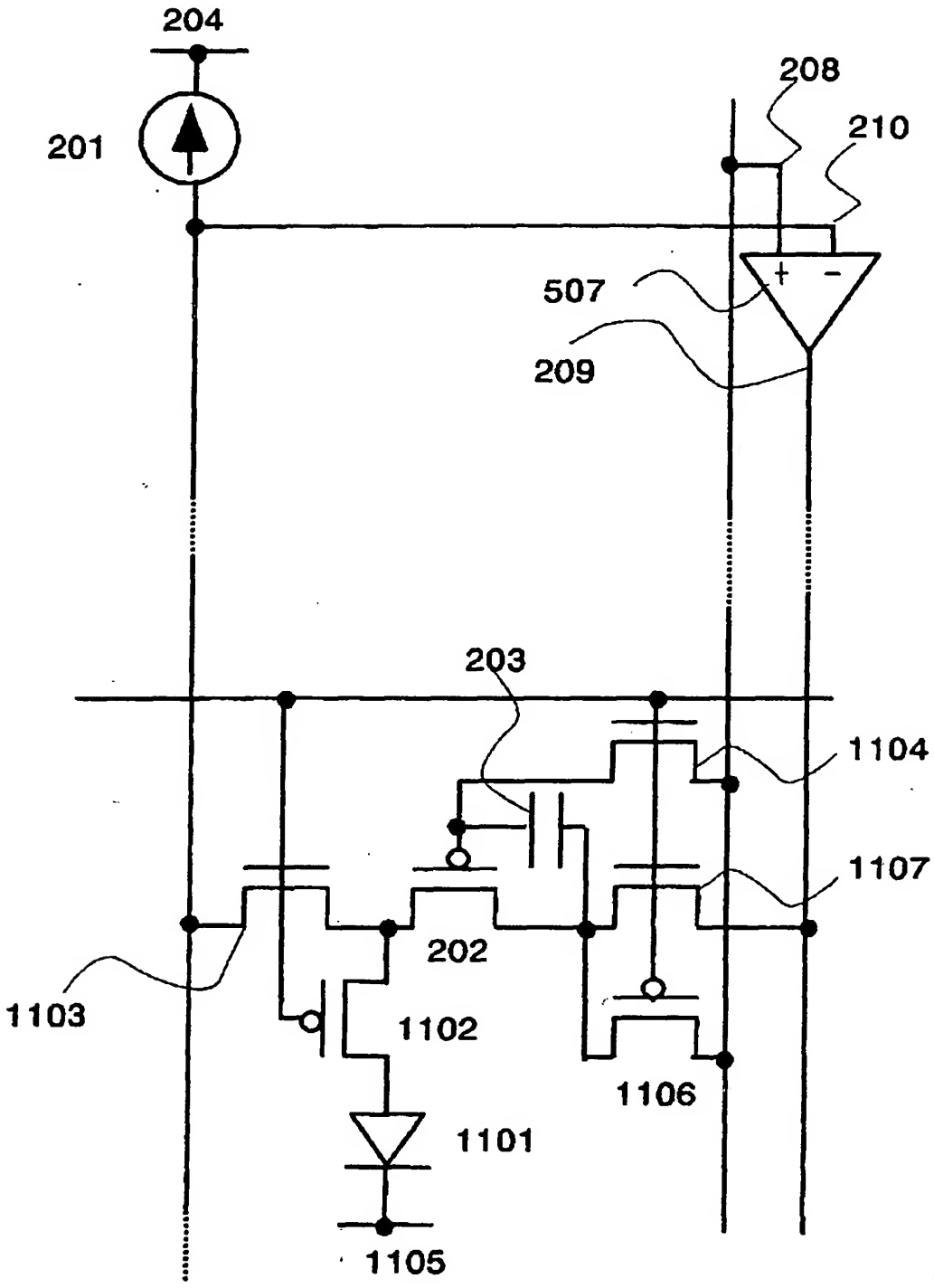
204
201
208
210
507
209
203
1104
1107
202
1103
1102
1106
1101
1105

FIG. 34

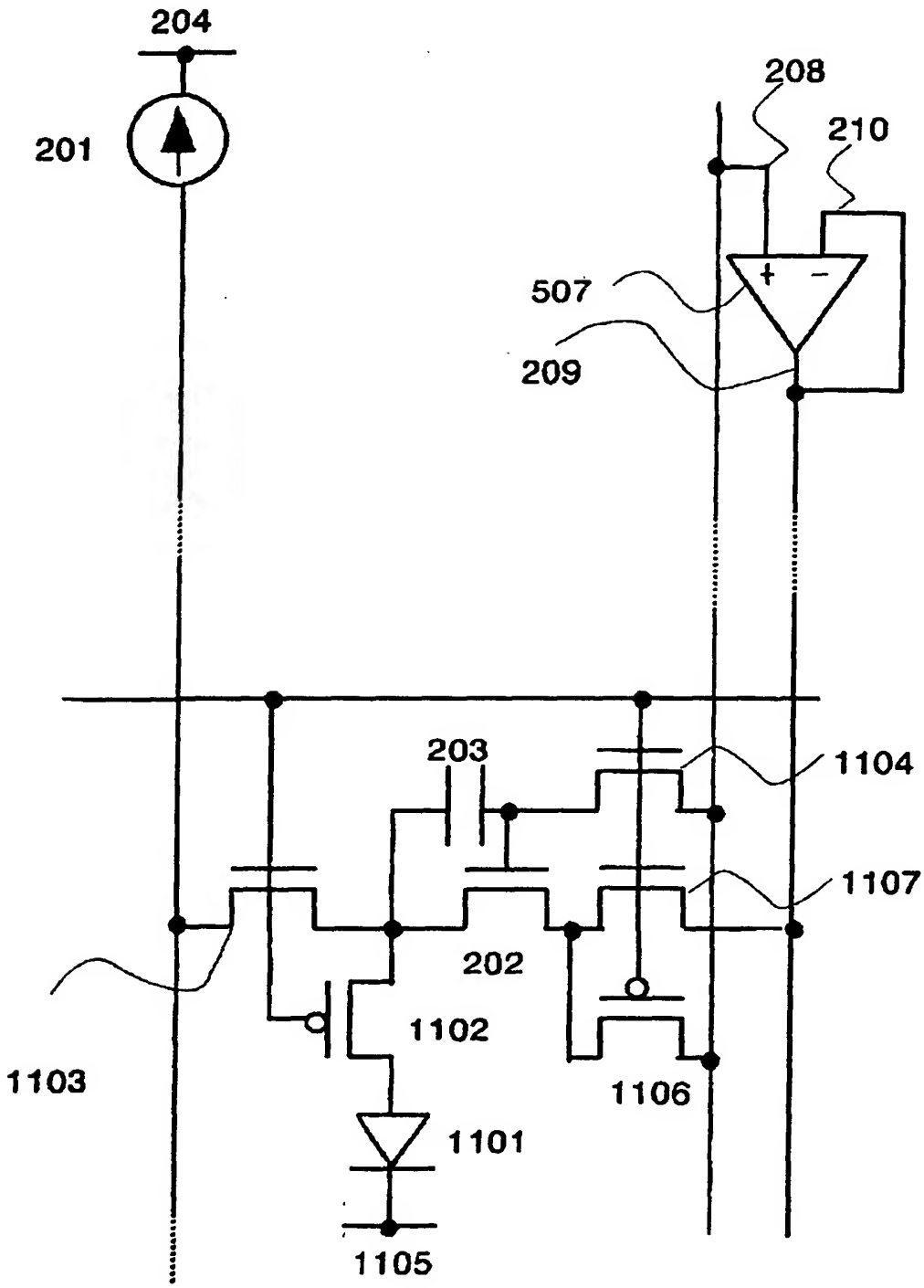
204
201
208
210
507
209
203
1104
1107
202
1102
1103
1106
1101
1105

FIG. 35

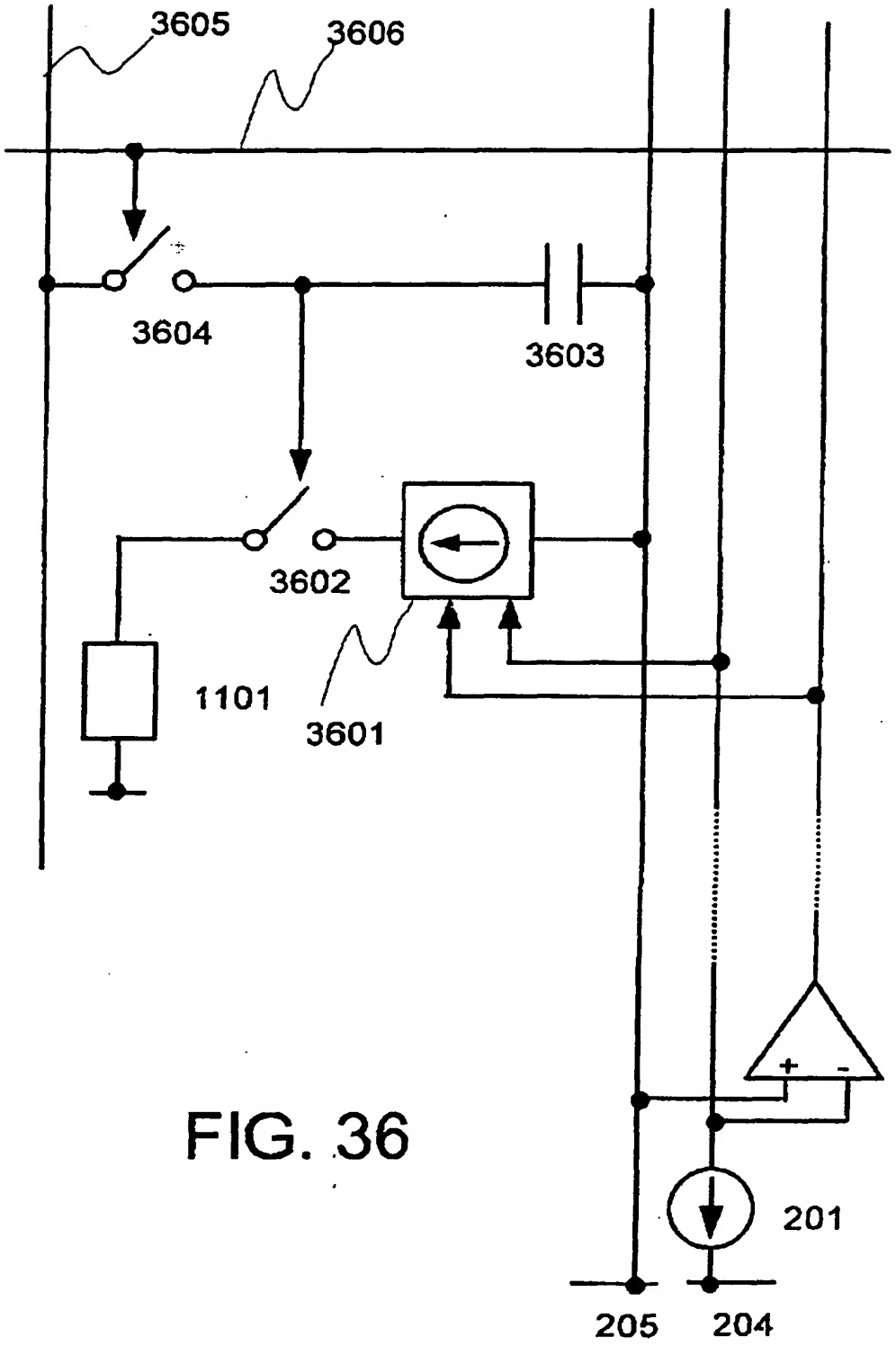

FIG. 36

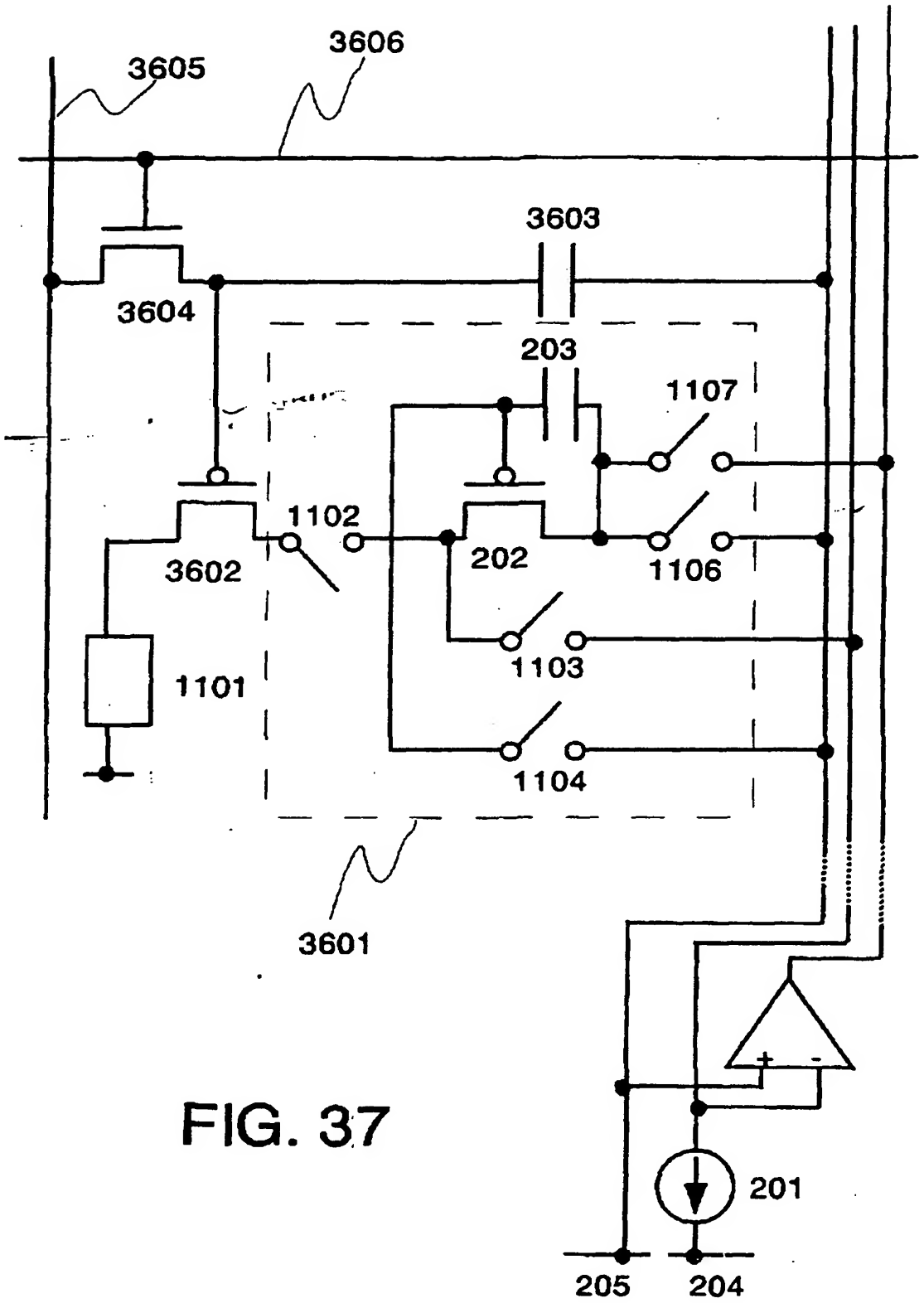
3605
3606
3603
3604
203
1107
1102
202
1106
3602
1103
1101
1104
3601
201
205
204

FIG. 37

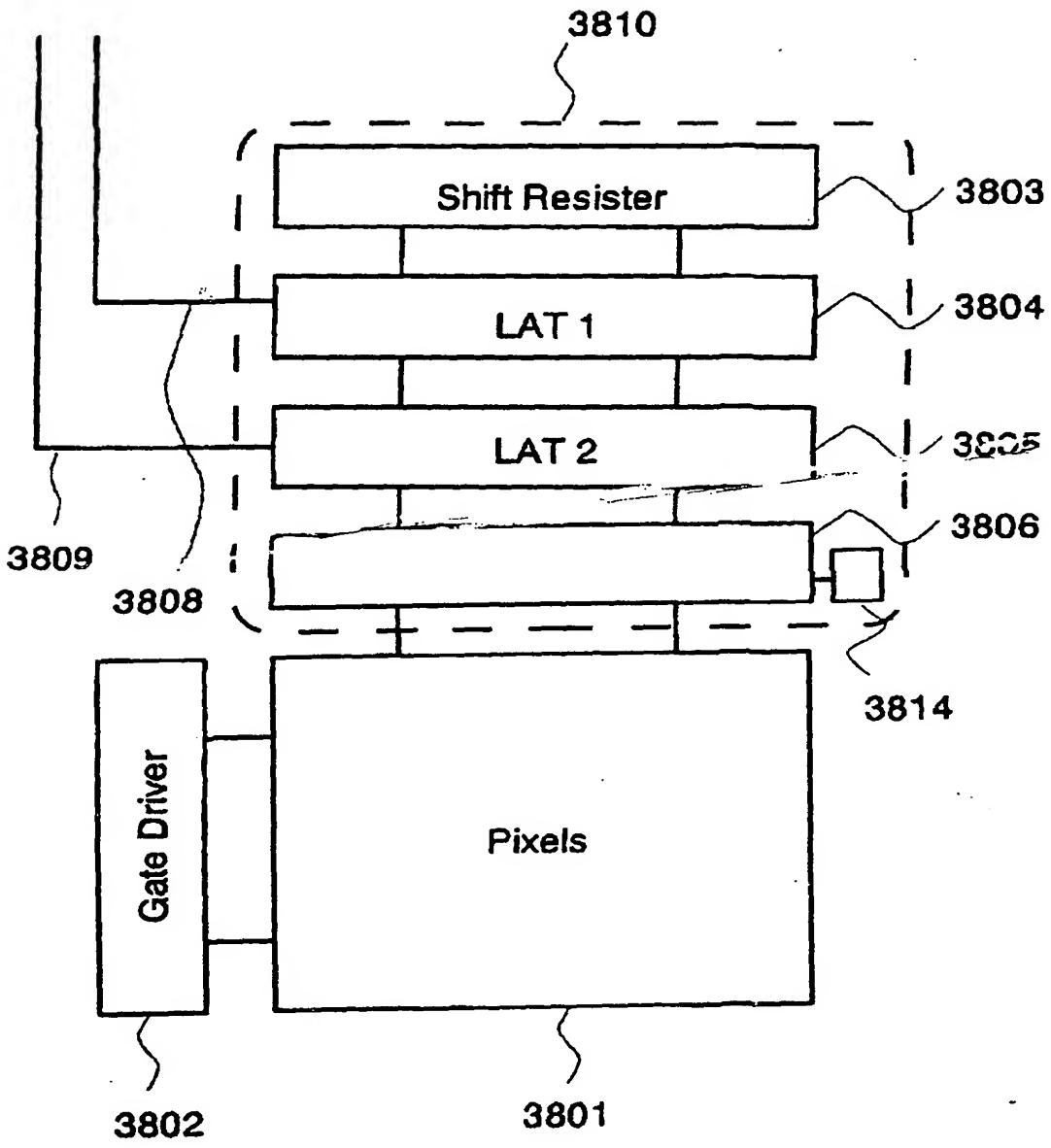
3810
Shift Resister
3803
LAT 1
3804
LAT 2
3805
3806
3809
3808
3814
Gate Driver
Pixels
3802
3801

FIG. 38

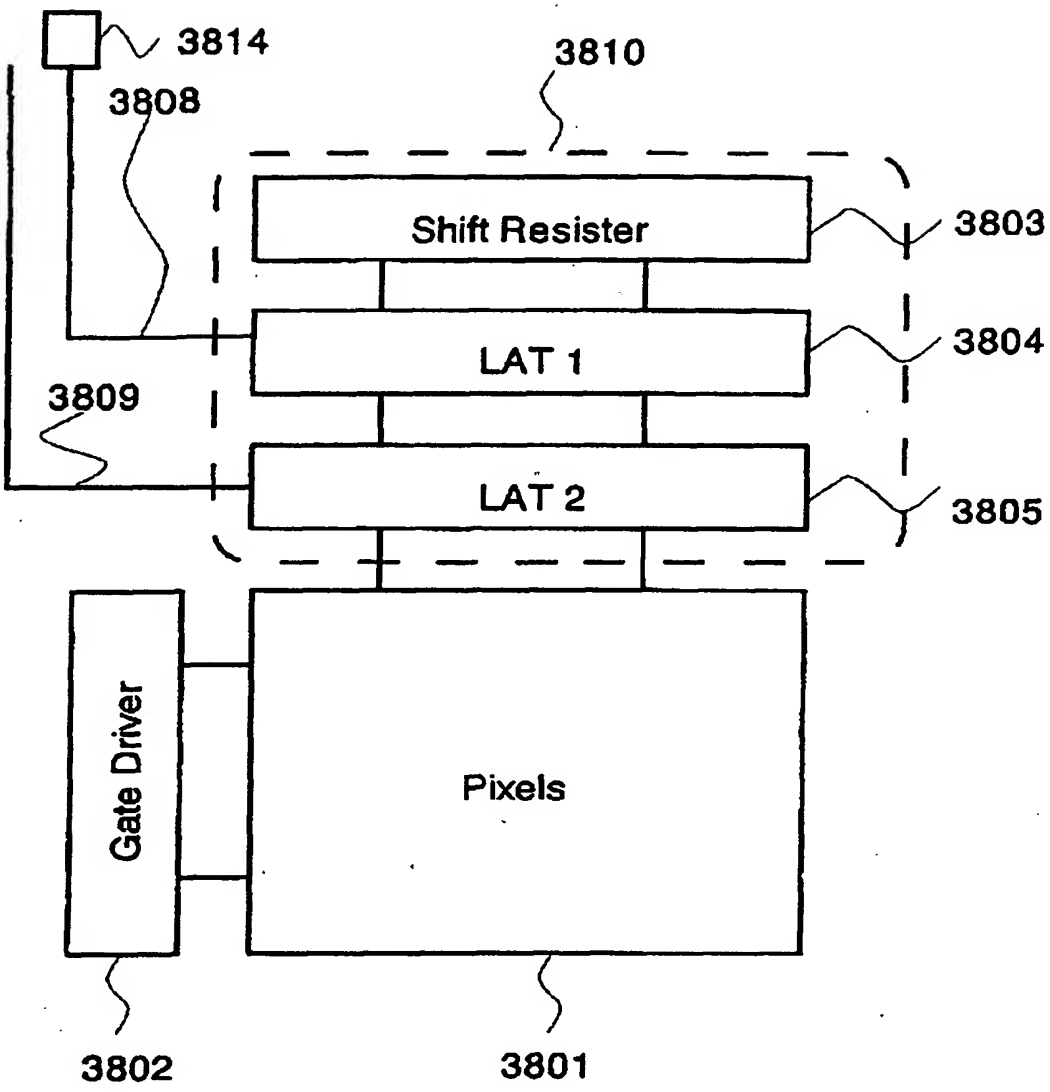
3814
3810
3808
Shift Resister
3803
LAT 1
3804
3809
LAT 2
3805
Gate Driver
Pixels
3802
3801

FIG. 39

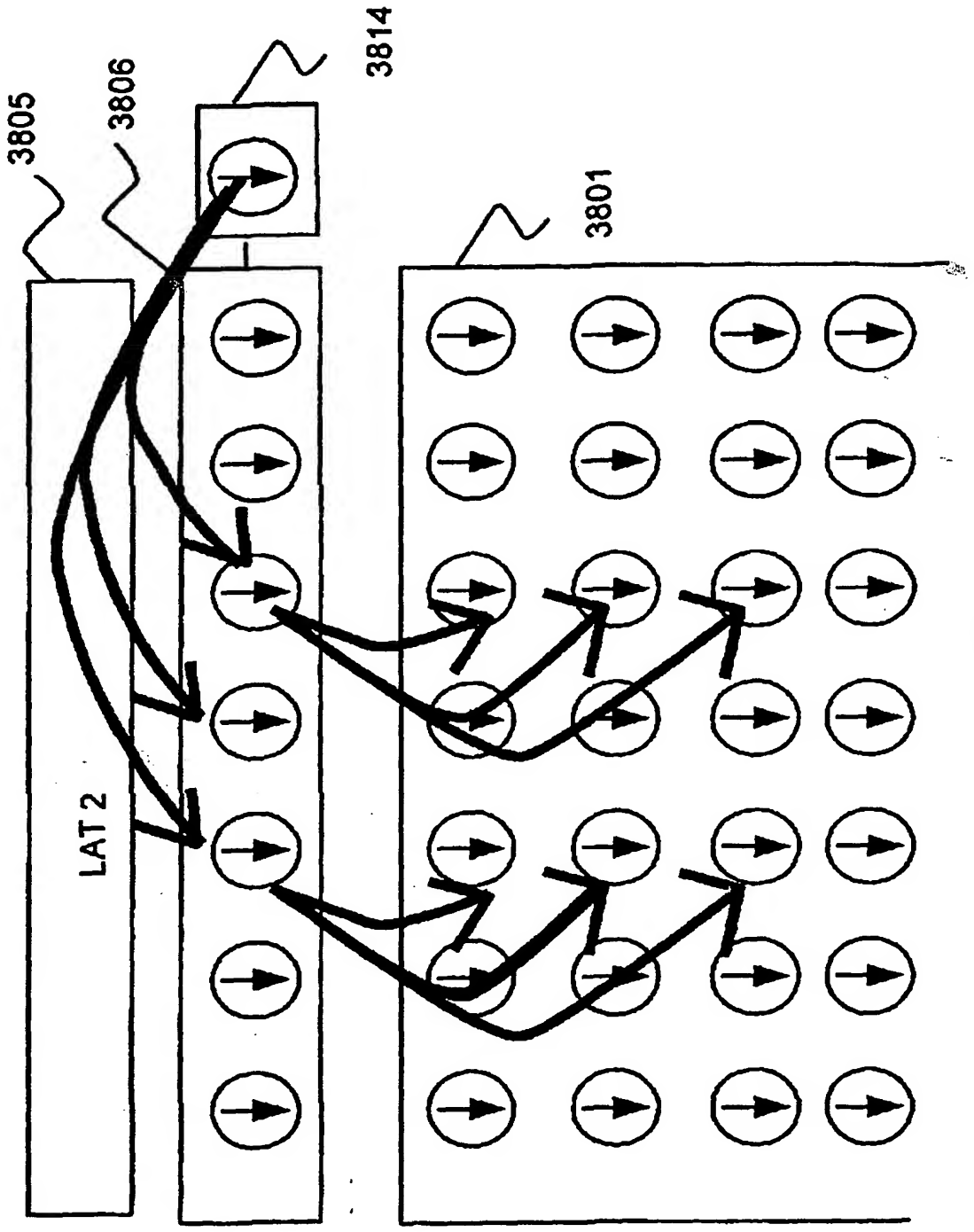

FIG. 40

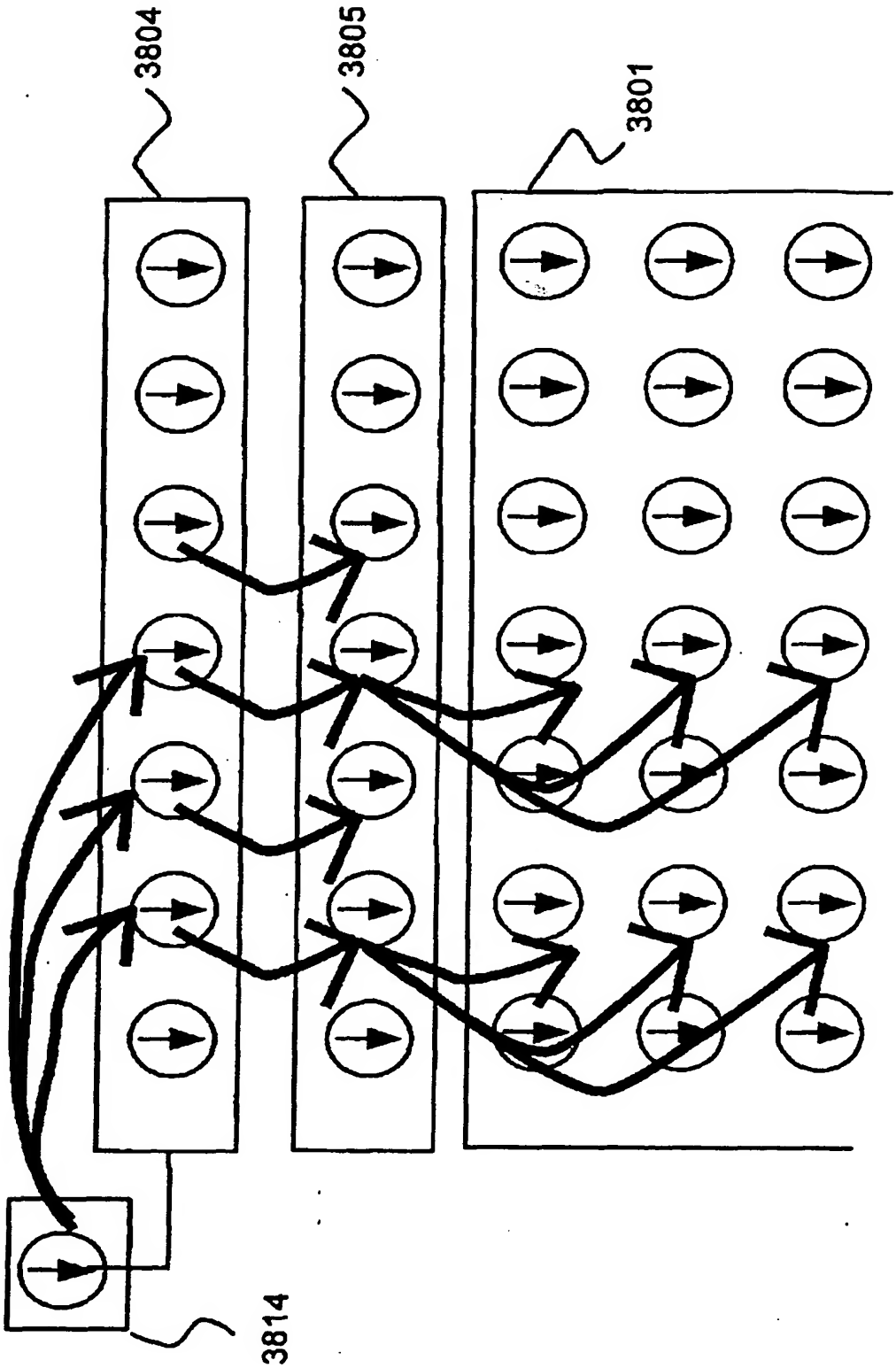

FIG. 41

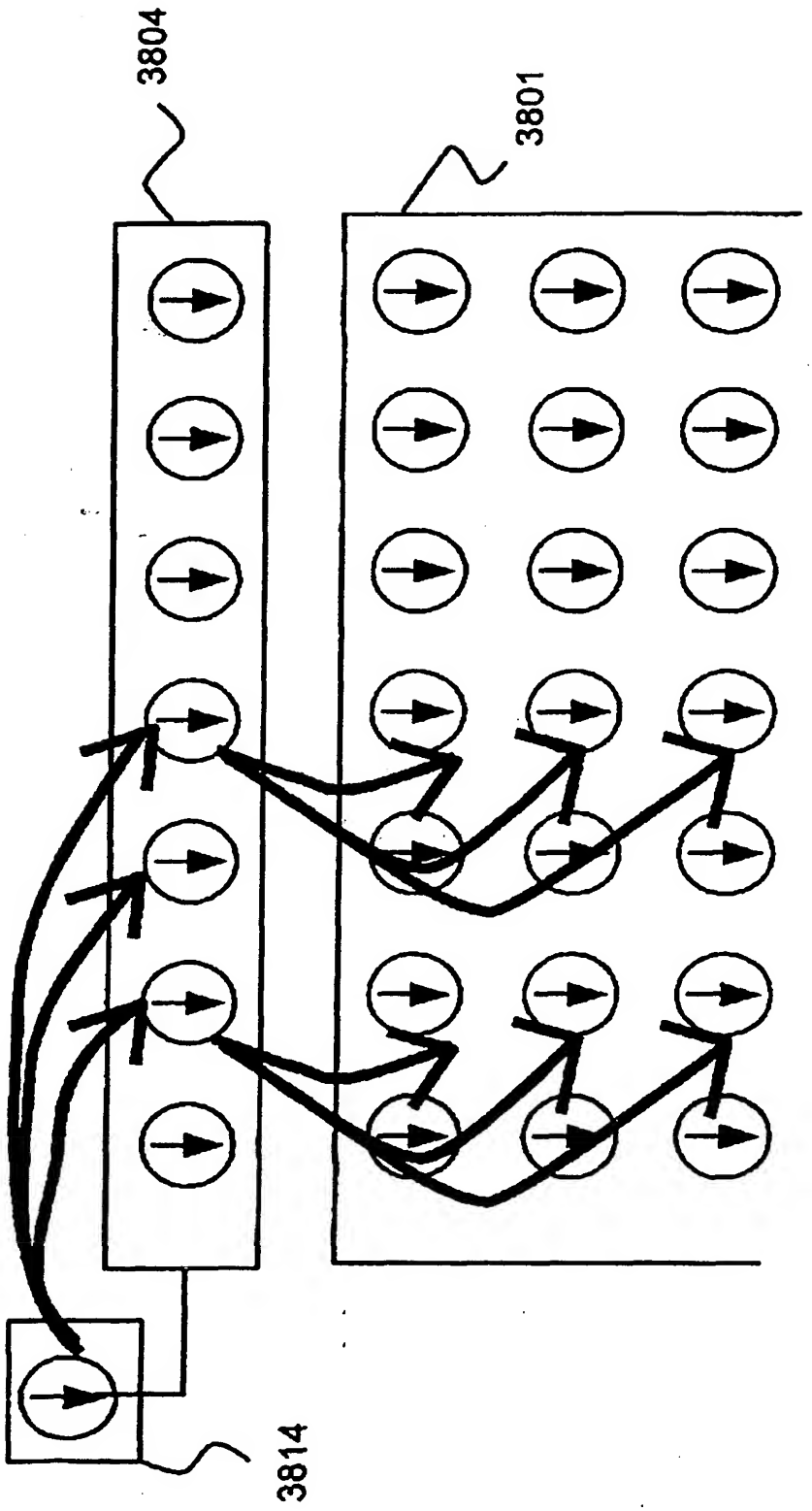

FIG. 42

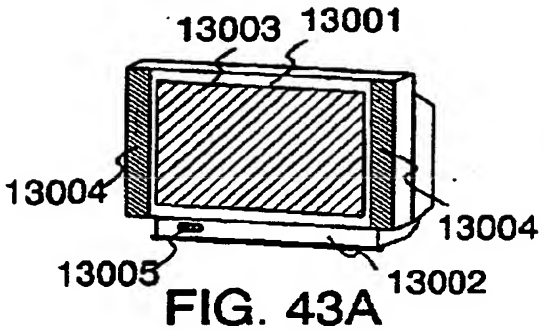

FIG. 43A

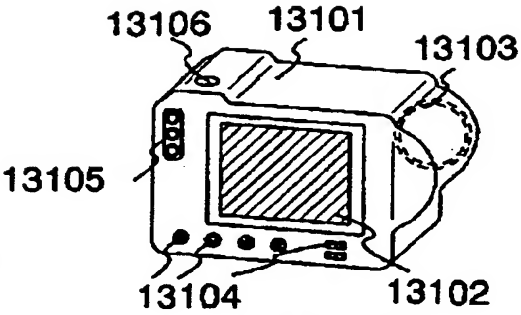

FIG. 43B

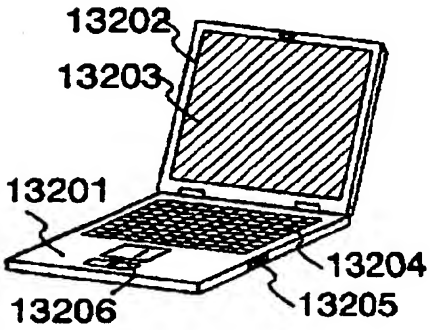

FIG. 43C

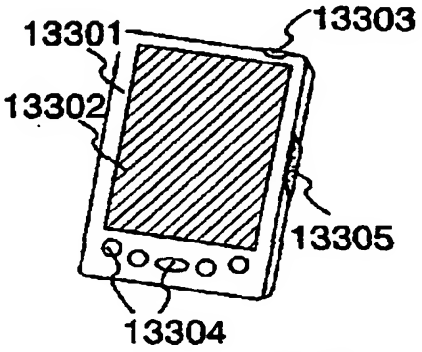

FIG. 43D

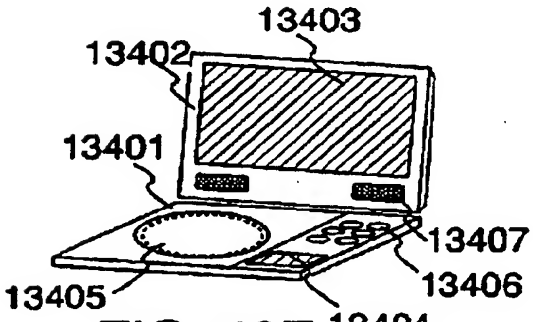

FIG. 43E

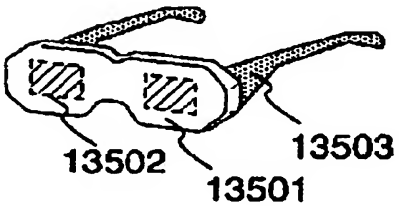

FIG. 43F

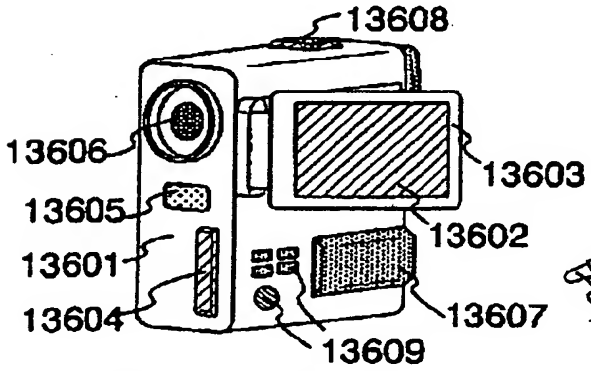

FIG. 43G

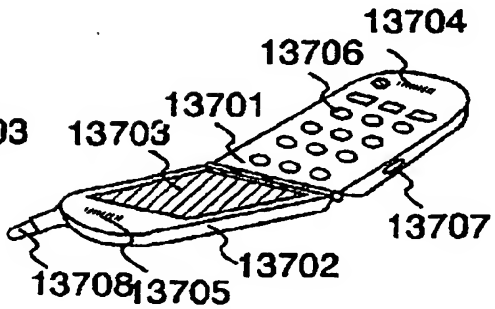

FIG. 43H

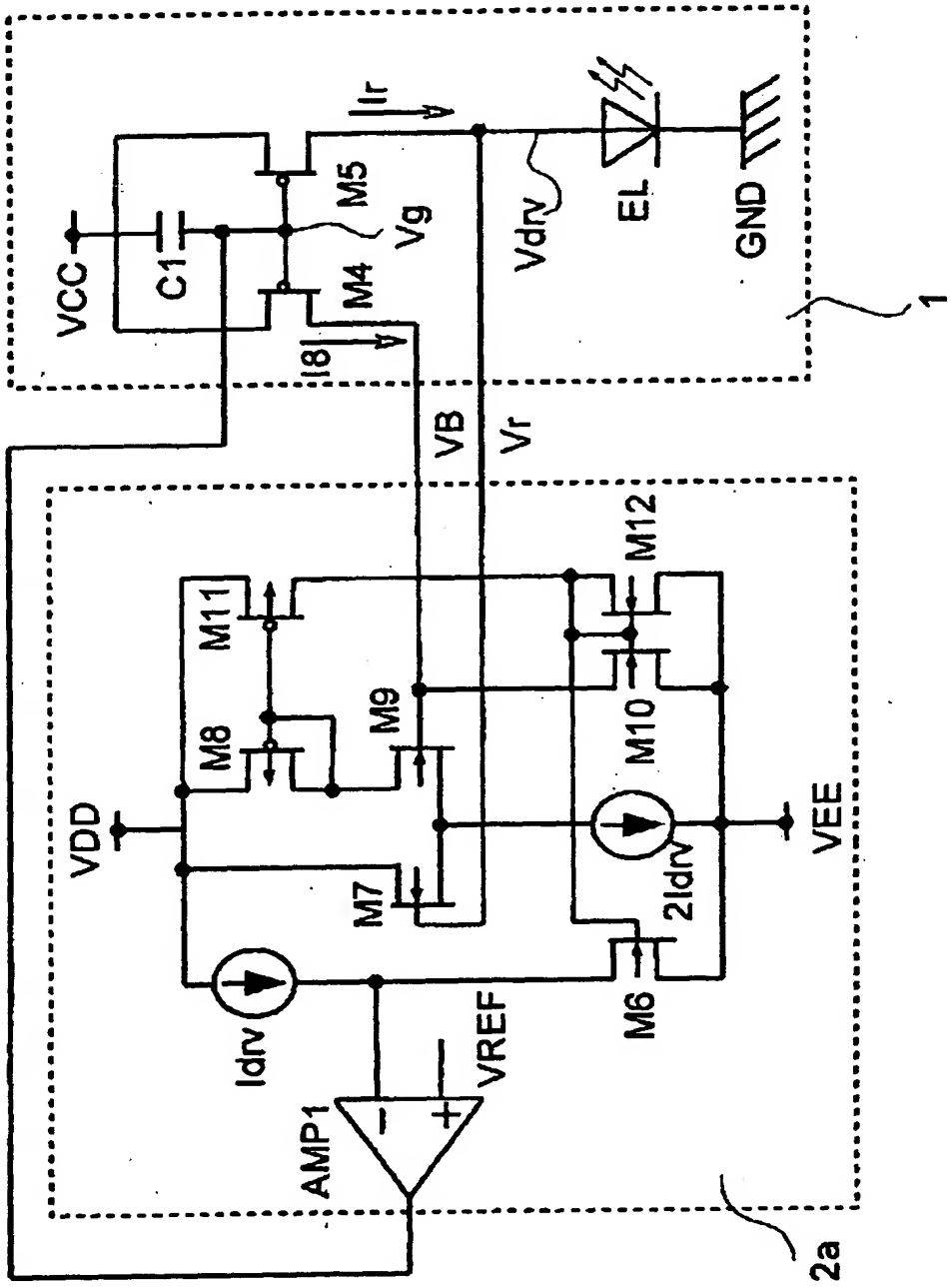
Ir
M5
Vg
Vdrv
EL
GND
VCC
C1
M4
I8
1
VB
Vr
M12
M11
M9
M10
M8
VDD
VEE
M7
2Idrv
Idrv
VREF
M6
AMP1
2a

FIG. 44

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2004/005969

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] G05F3/24

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] G05F3/24

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1922-1996	Toroku Jitsuyo Shinan Koho	1994-2004
Kokai Jitsuyo Shinan Koho	1971-2004	Jitsuyo Shinan Toroku Koho	1996-2004

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 11-149783 A (Hitachi, Ltd.), 02 June, 1999 (02.06.99), Fig. 1; Par. Nos. [0033] to [0037] (Family: none)	1-5,8-15
X	JP 2000-112548 A (Ricoh Co., Ltd.), 21 April, 2000 (21.04.00), Fig. 3; Par. Nos. [0002] to [0008] (Family: none)	6-15

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 August, 2004 (17.08.04)	31 August, 2004 (31.08.04)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (January 2004)